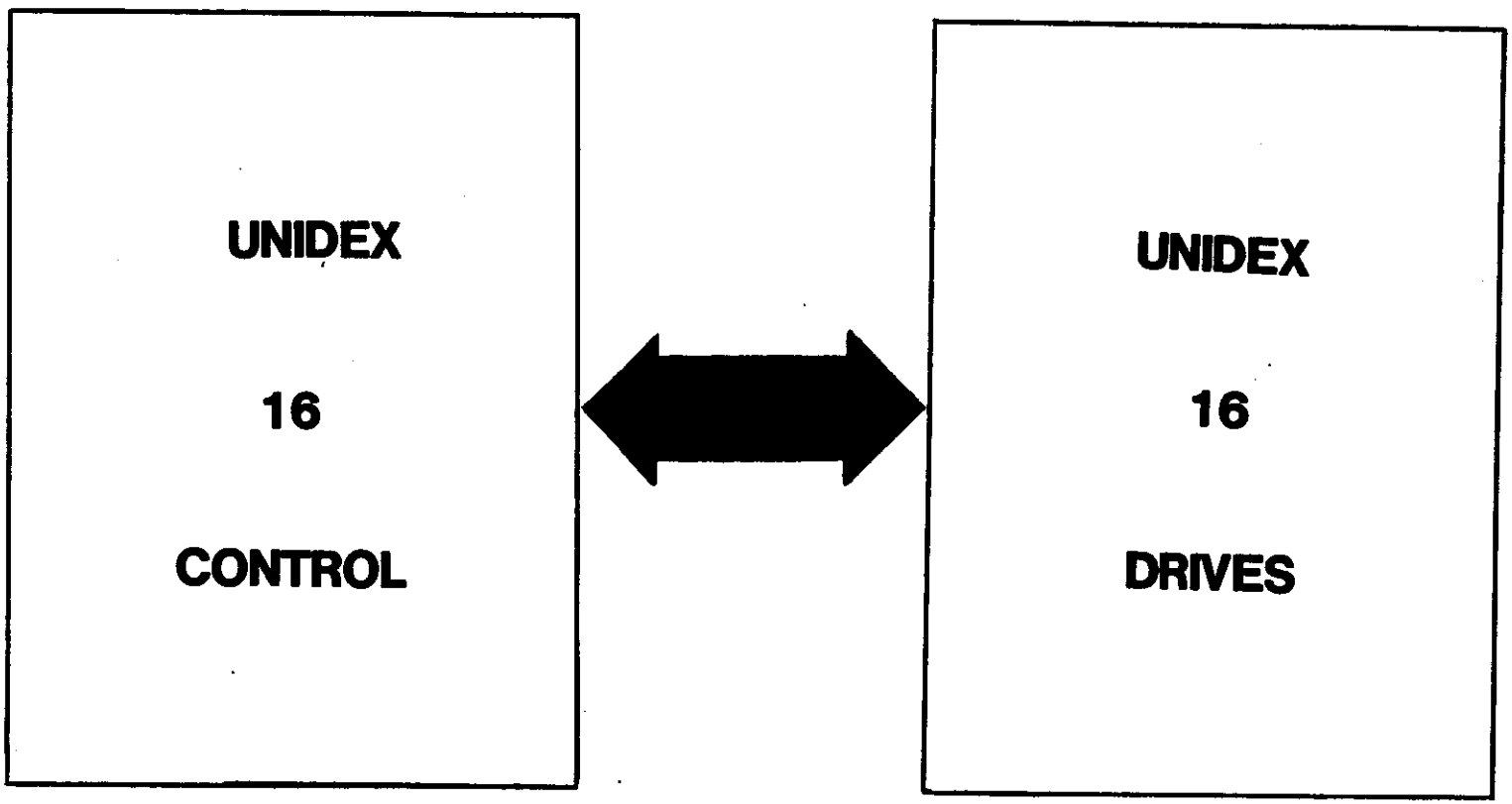
UNIDEX 16

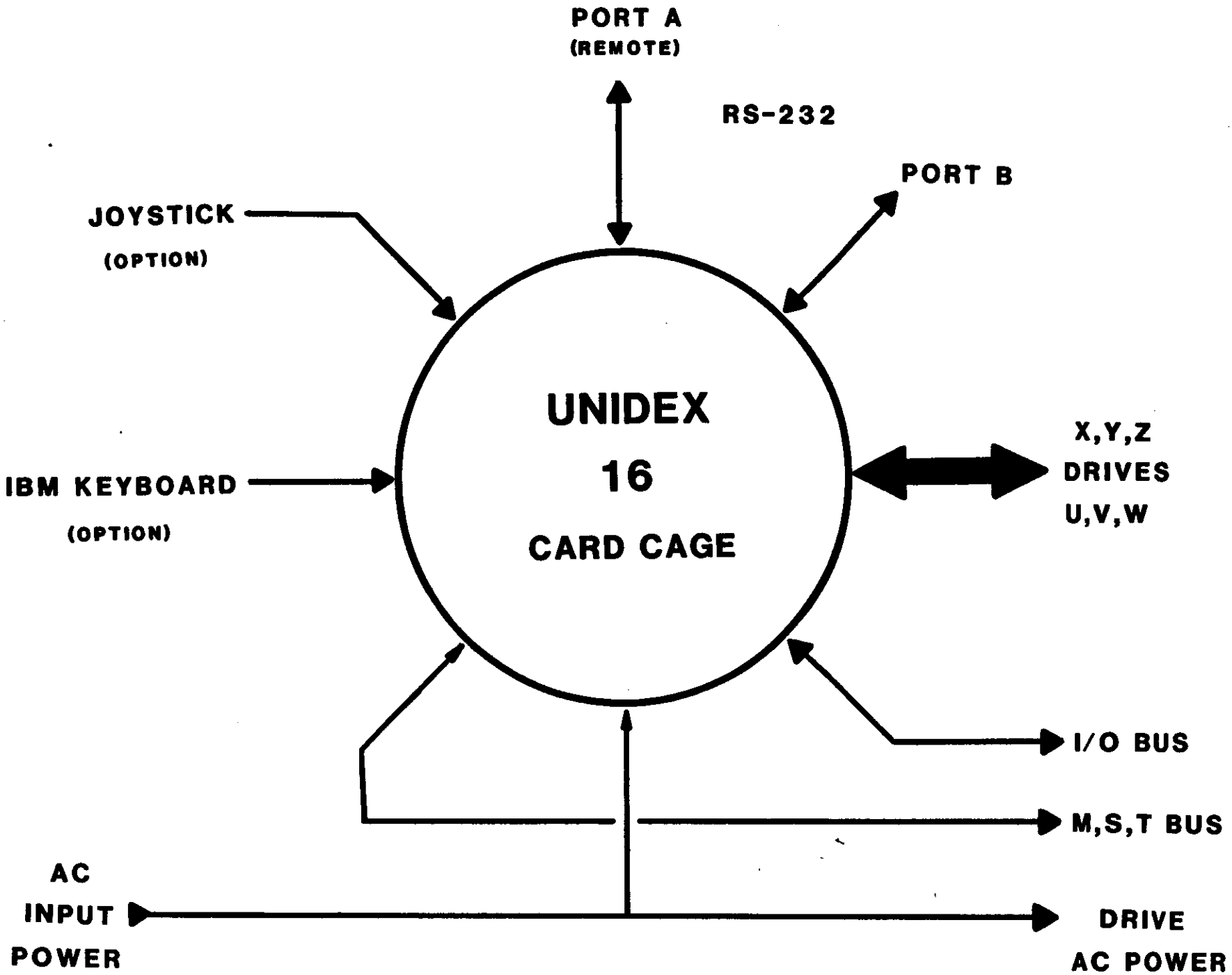
MAINTENENCE

CLASS

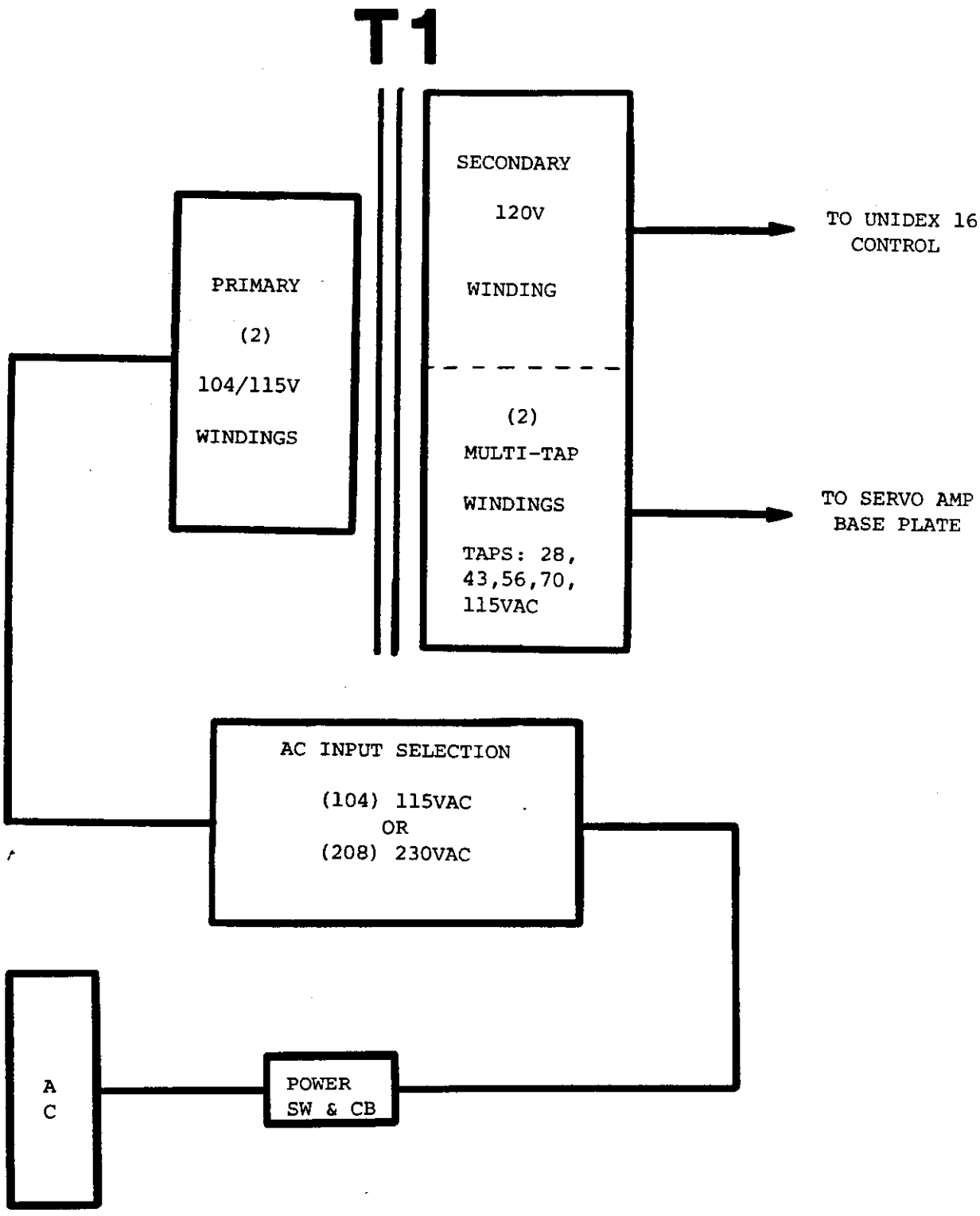
PART 1

MICRO SECTION


UNIDEX
16
CONTROL
UNIDEX
16
DRIVES

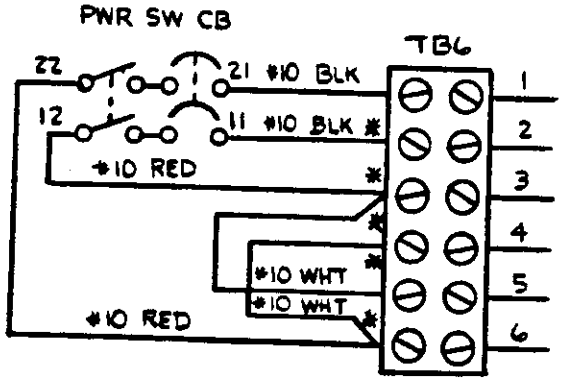

PORT A
(REMOTE)
RS-232
PORT B
JOYSTICK
(OPTION)
UNIDEX
16
CARD CAGE
IBM KEYBOARD
(OPTION)
X,Y,Z
DRIVES
U,V,W
I/O BUS
M,S,T BUS
AC
INPUT
POWER
DRIVE
AC POWER

AC POWER

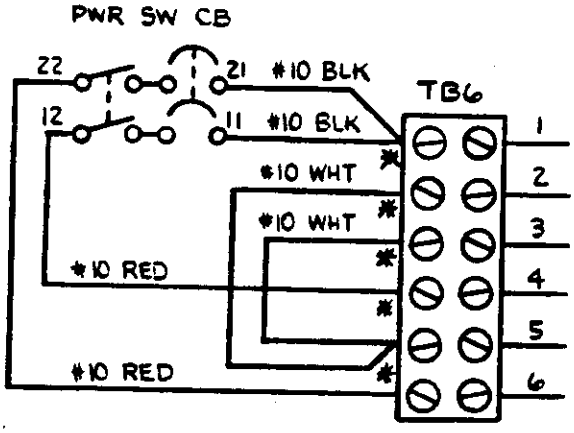


SINGLE PHASE

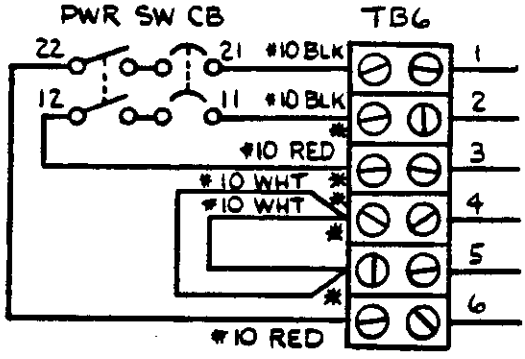
AC INPUT SELECTION



115VAC
10A / 15A



115VAC
20A / 30A



230VAC
15 A

* TB6 USES RING TONGUE LUGS
EXCEPT WHERE NOTED (*)
WHICH USES SPADE LUGS

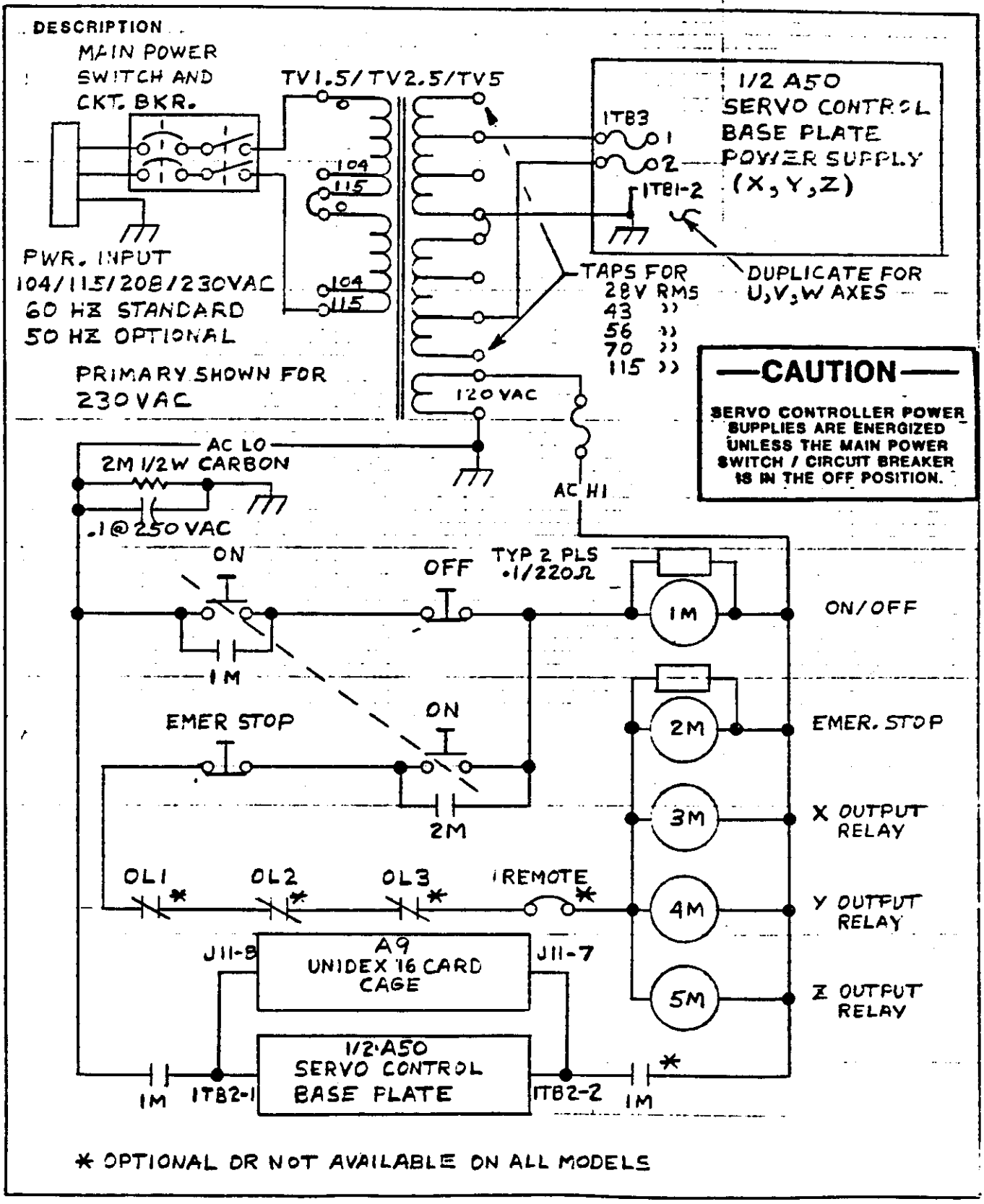
ENGINEERING SPECIFICATION ES11278 SHEET 1 OF 1

CUSTOMER _____ ORDER # _____

DATE 4/2/96 REV Ø BY JLD CHK _____

SUBJECT FUNCTIONAL AC POWER WIRING FOR UNIDEX 16 SYSTEMS

DESCRIPTION



—CAUTION—

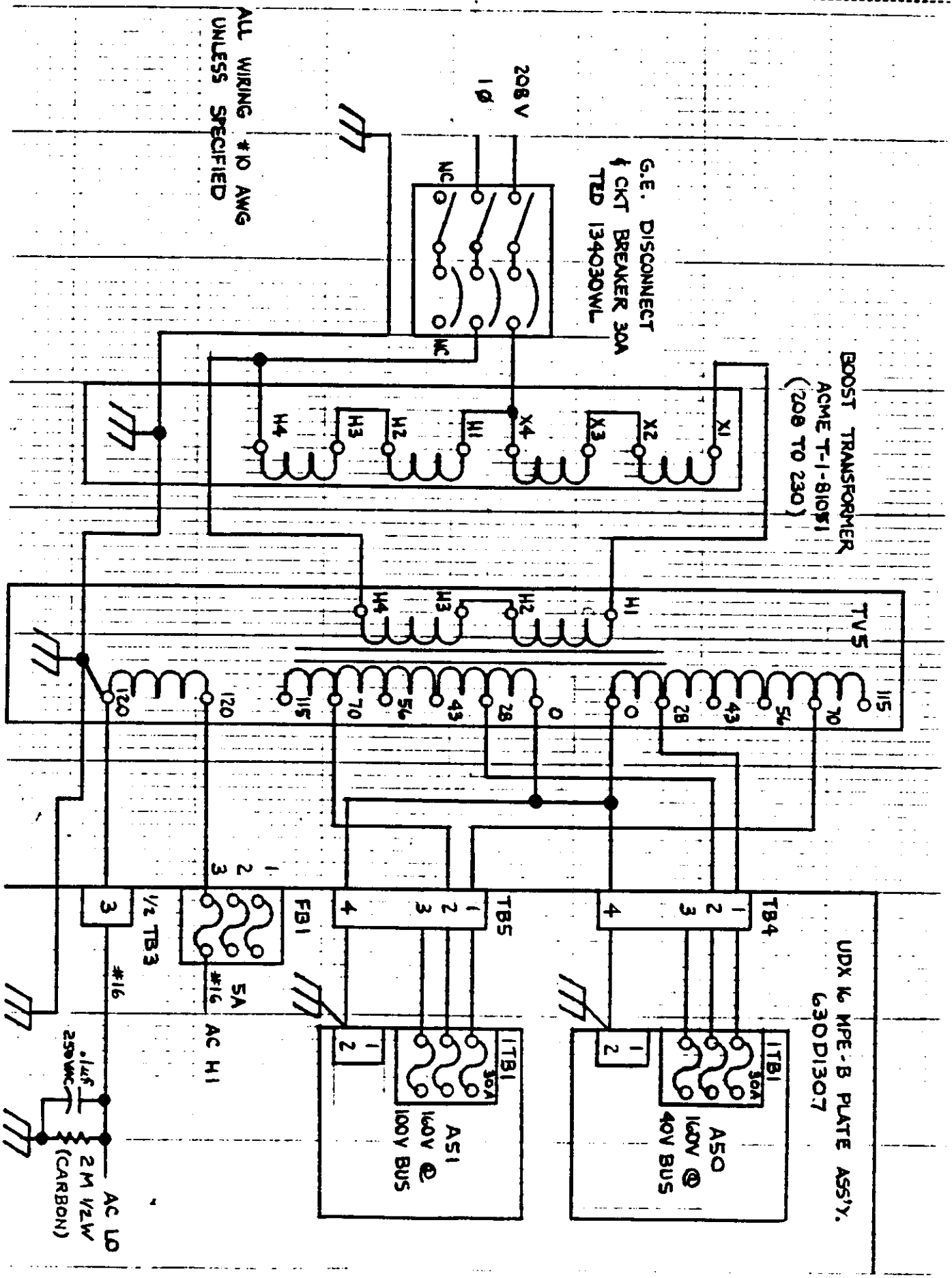
SERVO CONTROLLER POWER SUPPLIES ARE ENERGIZED UNLESS THE MAIN POWER SWITCH / CIRCUIT BREAKER IS IN THE OFF POSITION.

* OPTIONAL OR NOT AVAILABLE ON ALL MODELS

BY D. SAGATH DATE 10/29/85
CHKD. BY ..... DATE .....

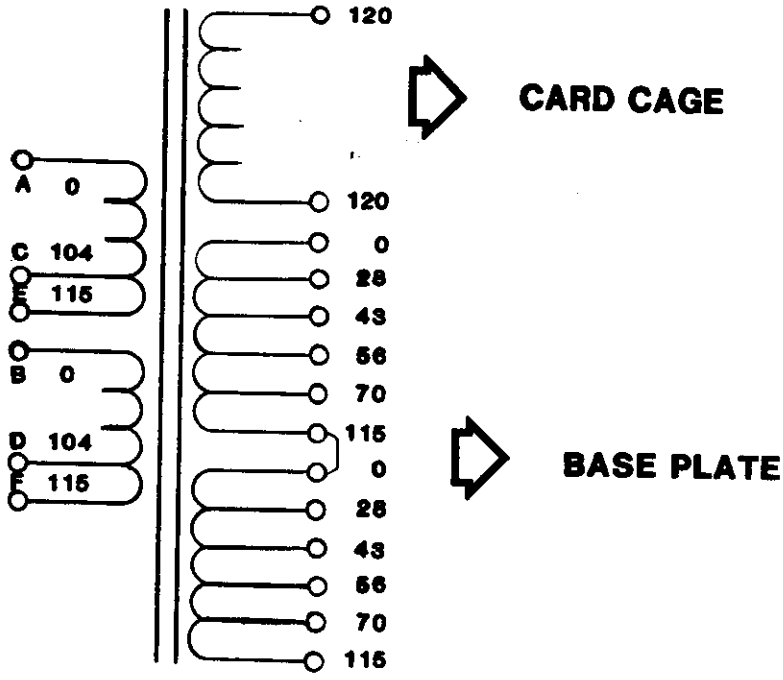
SUBJECT AC POWER WIRING
TV5 / BOOST TRANSFORMER
USED ON SN 2248201/5

SHEET NO. 1 OF 1
JOB NO. ASK 22482-9



T1

TV2.5/TV5A

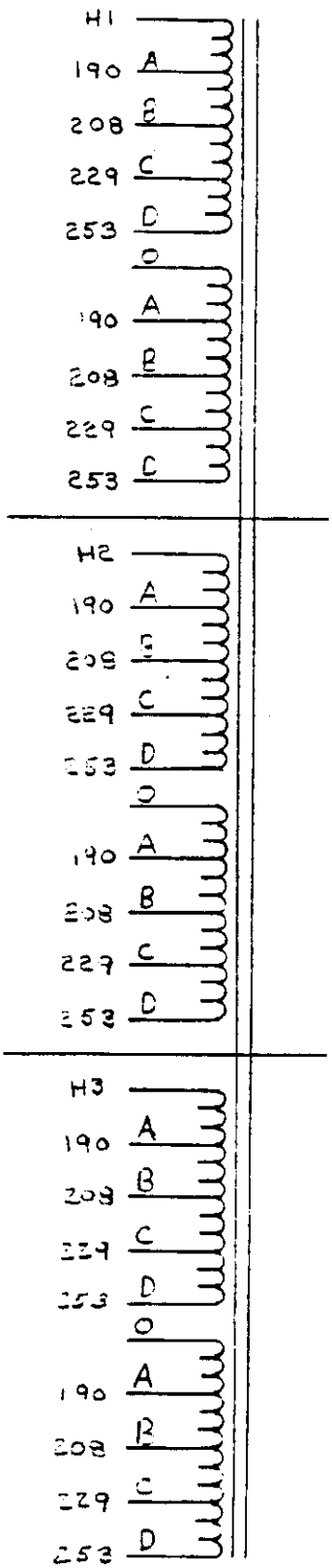

120
CARD CAGE
120
A 0
C 104
E 115
0
28
43
56
70
115
B 0
D 104
F 115
0
28
43
56
70
115
BASE PLATE

BY T. Martin DATE 5/24/23
CHKD. BY ____ DATE ____

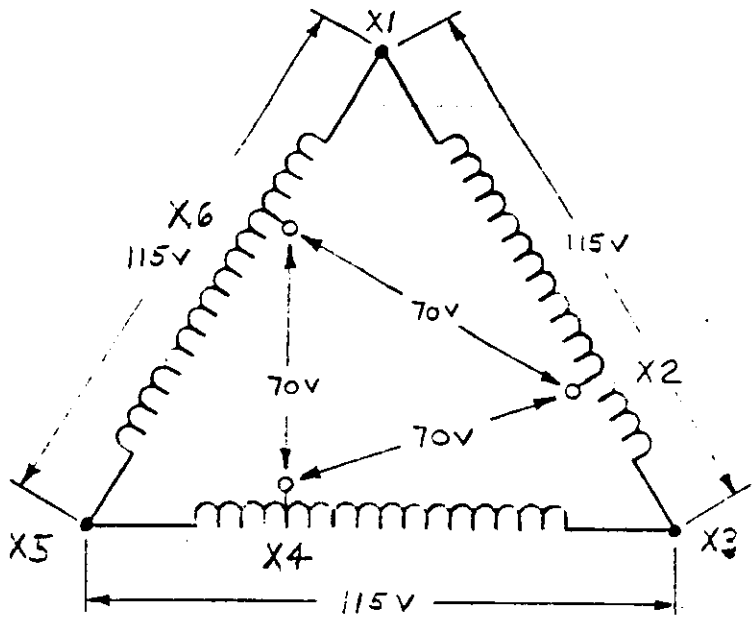
SUBJECT SPEC. CONTROL DWG. FOR 3Ø TRANSFORMER 60HZ (EA2-20)

SHEET NO. 1 OF 2
JOB NO. 60224010
REV A

DUAL PRIMARY
230/460
WITH TAPS FOR:

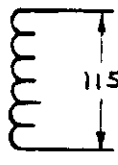


SECONDARY

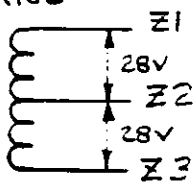


115V 3Ø DELTA @ 6KVA
70V 3Ø DELTA @ 6KVA

ALSO



AND



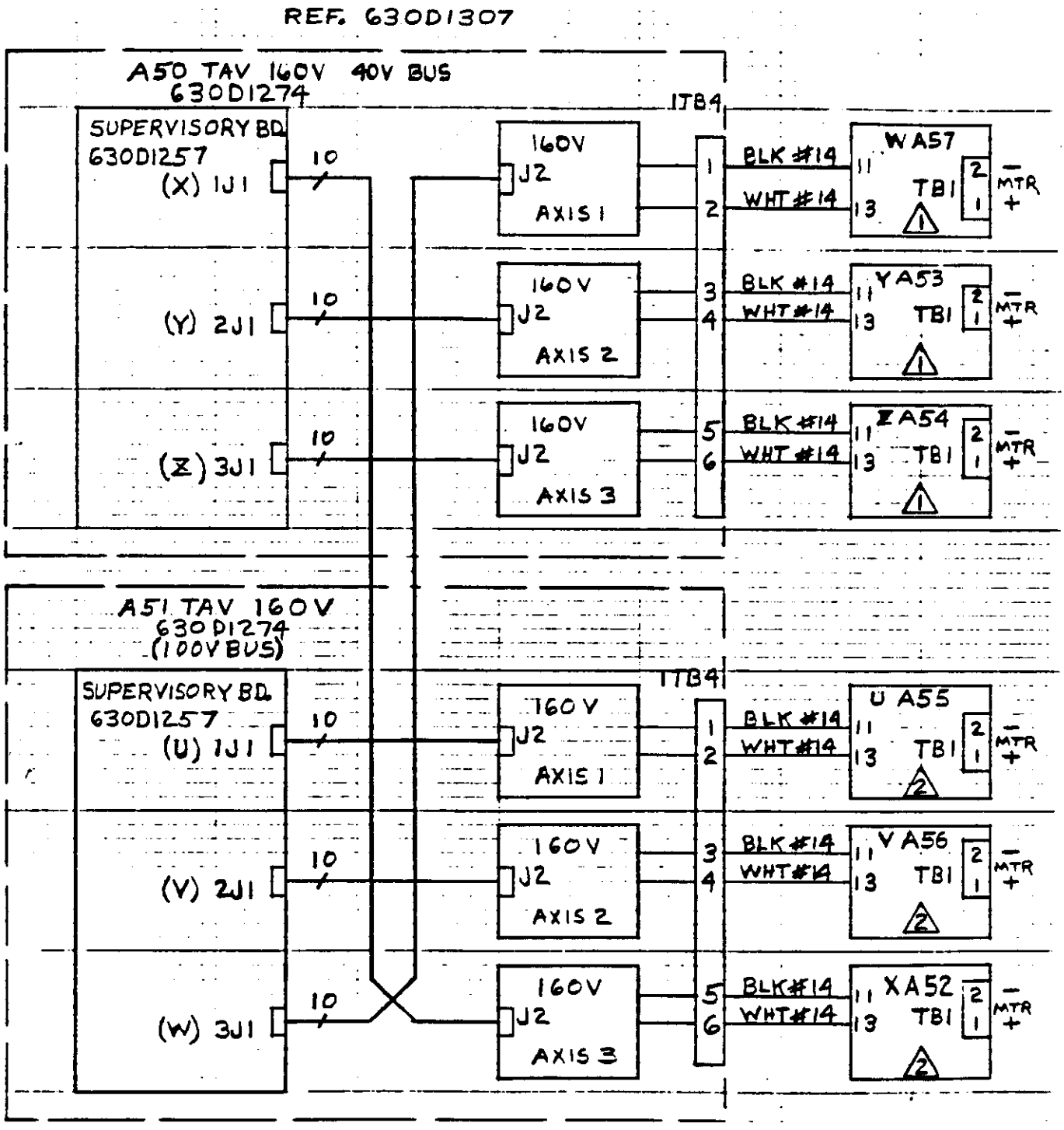
56V CT @ 500VA

2KVA PEAK

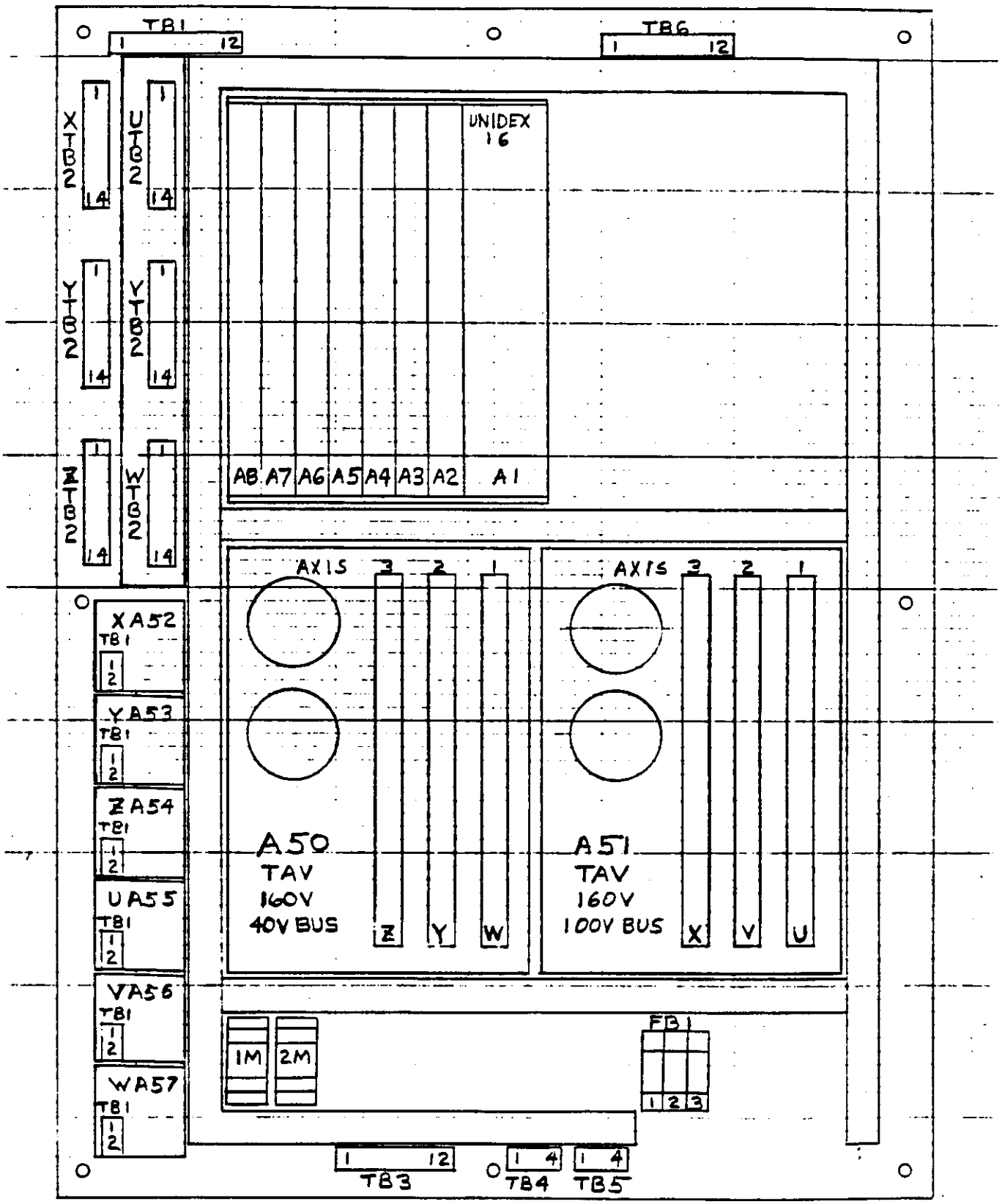
41 TERMINALS TOTAL

5% REGULATION

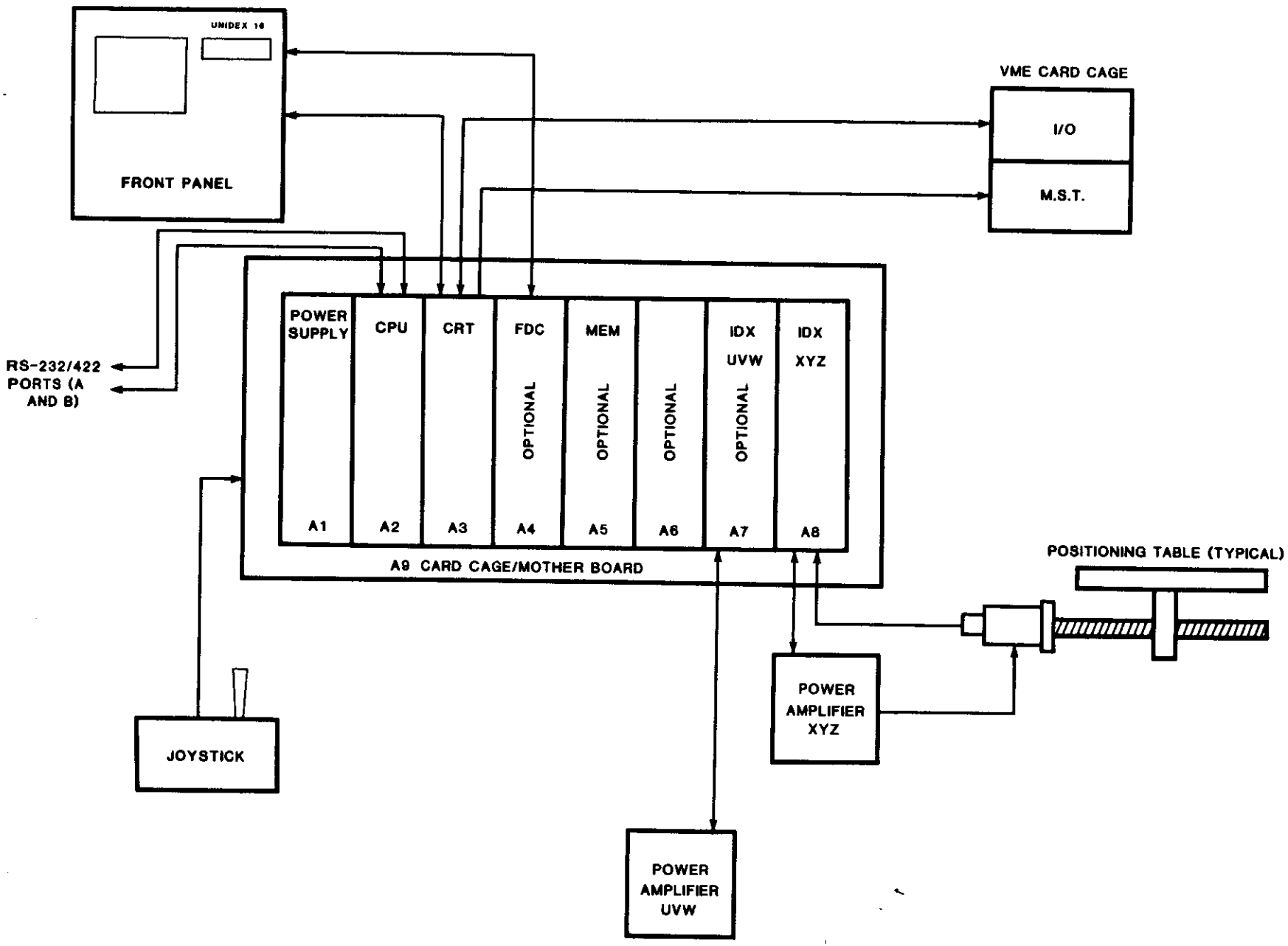
180°C


REF. 630D1307
A50 TAV 160V 40V BUS
630D1274
ITB4
SUPERVISORY BD
630D1257
(X) 1J1
(Y) 2J1
(Z) 3J1
10
160V
J2
AXIS 1
AXIS 2
AXIS 3
1
2
3
4
5
6
BLK #14
WHT #14
W A57
Y A53
Z A54
11
13
TB1
2
1
MTR
+
A51 TAV 160V
630D1274
(100V BUS)
ITB4
SUPERVISORY BD
630D1257
(U) 1J1
(V) 2J1
(W) 3J1
160V
U A55
V A56
X A52

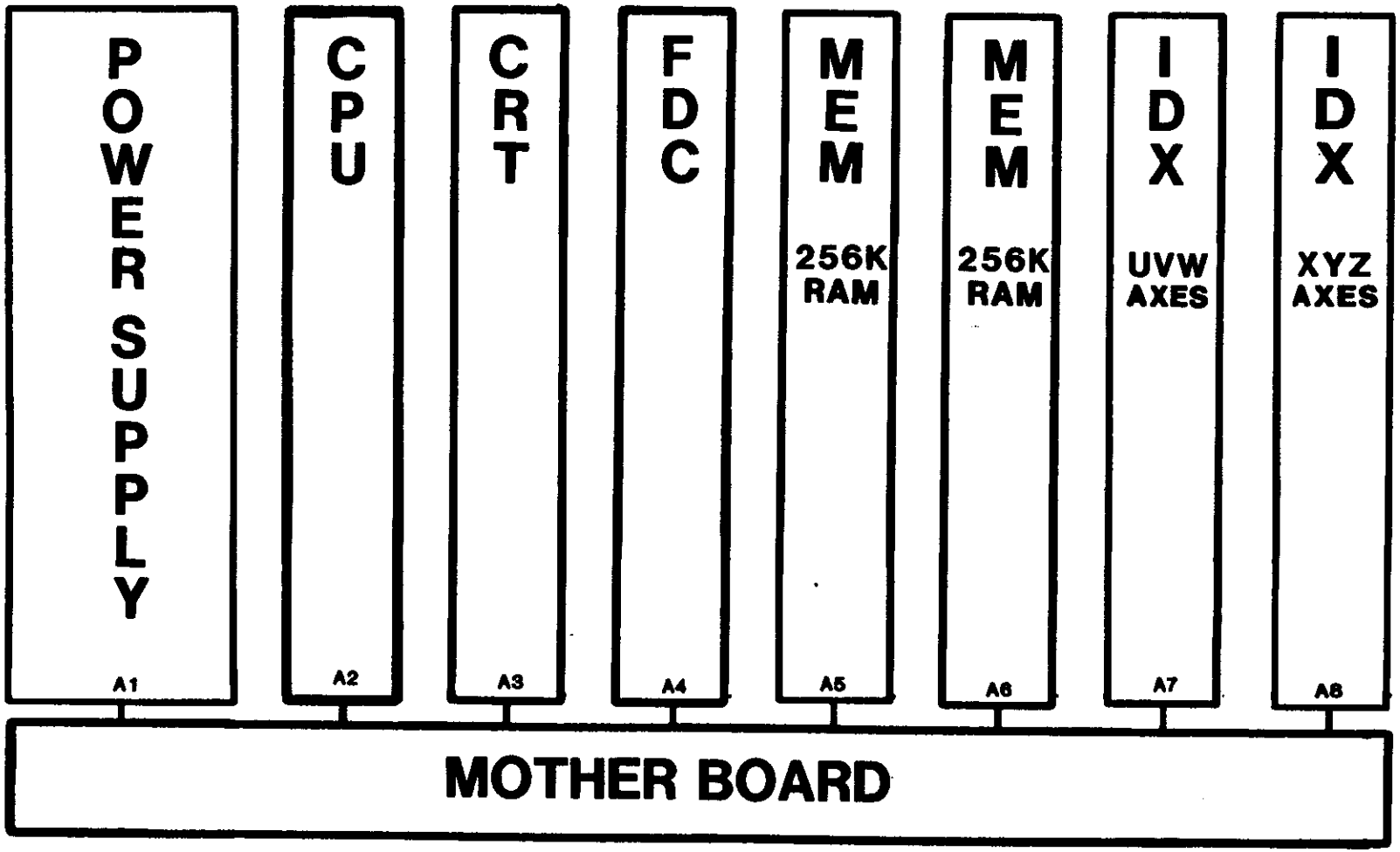
HOFFMAN A48P36



UNIDEX 16 HARDWARE

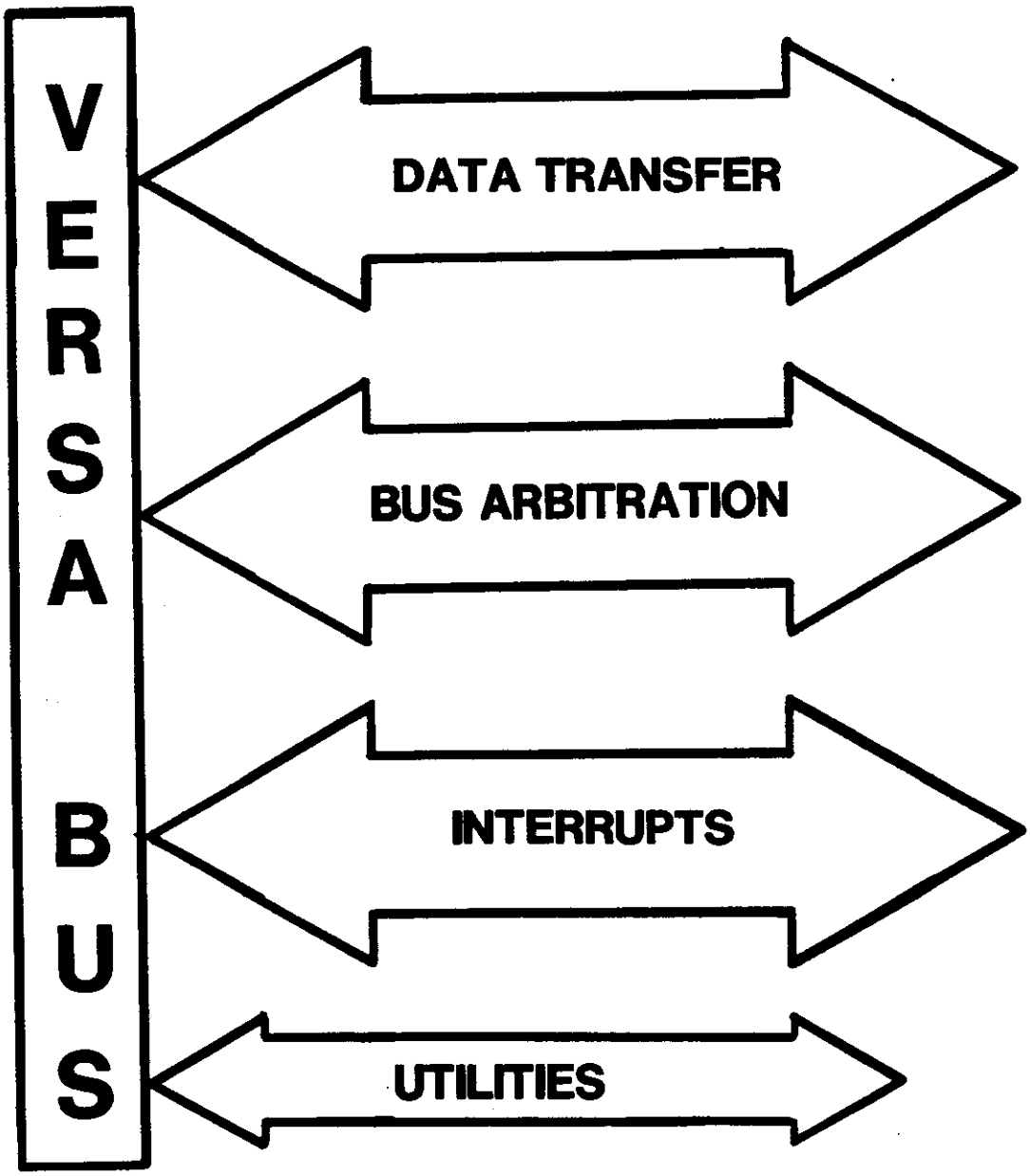


UNIDEX 16 CARD CAGE



CARD CAGE

VERSABUS


VERSA BUS
DATA TRANSFER
BUS ARBITRATION
INTERRUPTS
UTILITIES

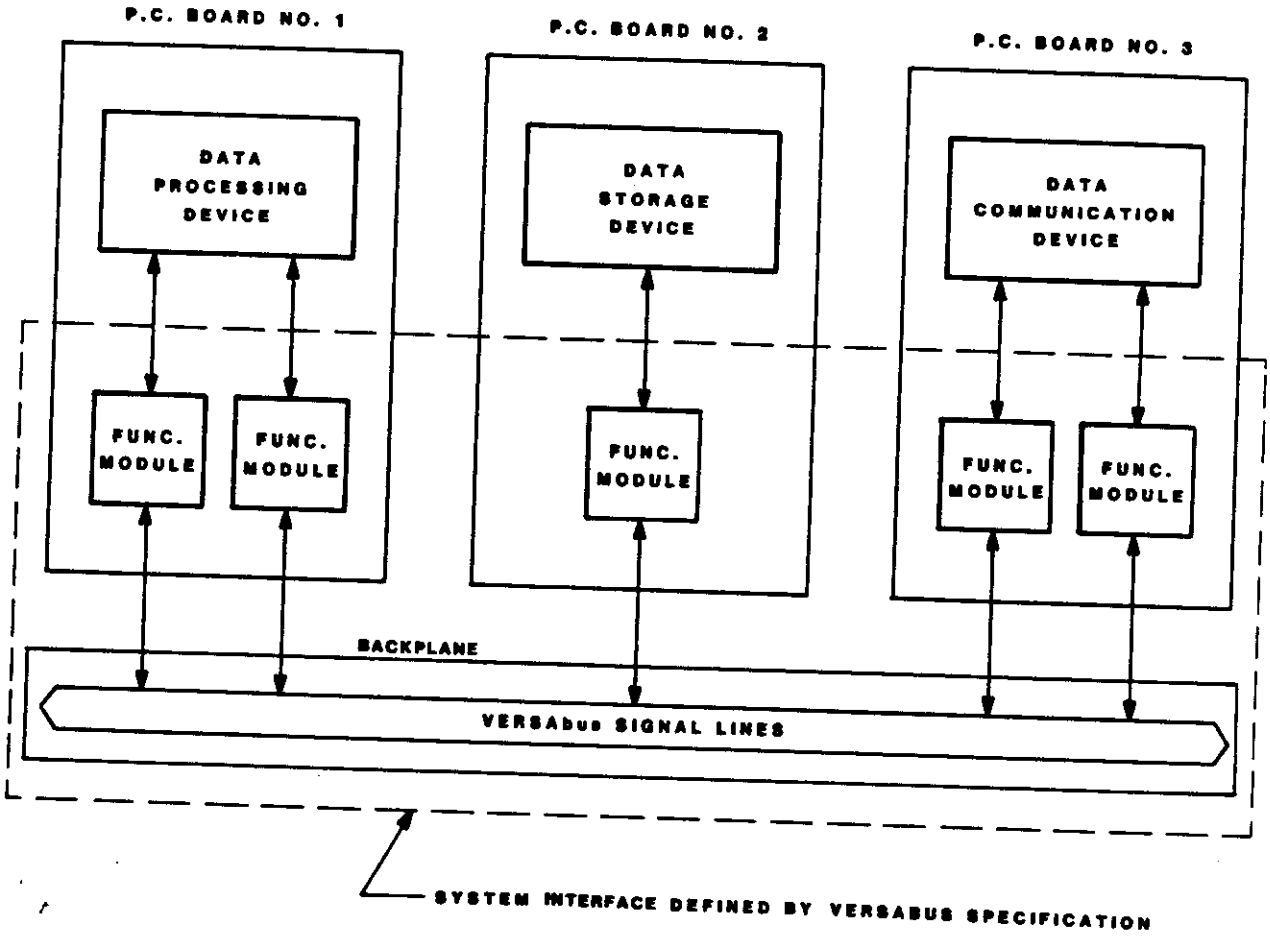


FIGURE 1-2. System Elements Defined by the VERSAbus Specification

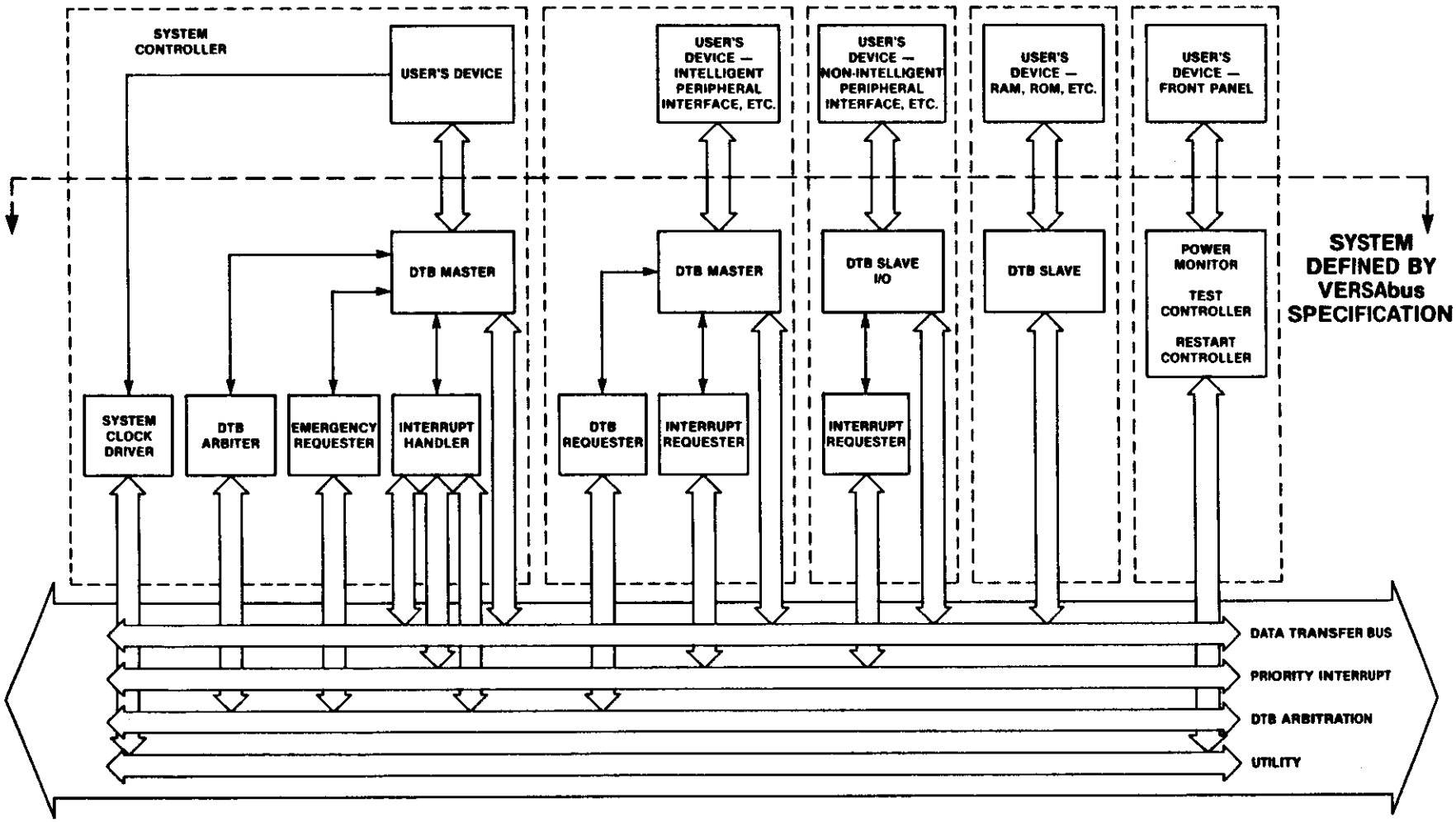


FIGURE 1-3. Functional Modules and Buses contained within the VERSAbus Definition

TABLE 1-1. VERSAbus Signal Line Terminology

SIGNAL LINE CATEGORY	SIGNAL LINE MNEMONICS (1)	TERMINOLOGY		
		OUTPUT	INPUT	ASTERISK
BUS LINES (Three-state)	A01*-A31* D00*-D31* APARITY0*-APARITY1* DPARITY0*-DPARITY3* AM0*-AM7* TEST0*-TEST1* WRITE*, LWORD*	Drive X Drive X high Drive X low Place valid X Remove X Release X	Receive X driven high Receive X driven low Receive X	Indicates a low level Equals a logic 1
Drive X defines the point at which the three-state drivers are enabled. Place valid X defines the point at which the levels on the bus are valid. Remove X defines the point at which the levels on the bus are invalid. Release X defines the point at which the three-state drivers are no longer enabled.				
STROBE LINES (Three-state)	AS* DS0* DS1*	Drive X to low Drive X to high	Receive X driven to low Receive X driven to high	Indicates the information on the strobed bus is valid on the falling edge of the strobe line.
STROBE RESPONSE LINES (Open Collector)	DTACK* BERR*	Drive X to low Release X to high	Receive X driven to low Receive X high	Indicates the strobe response is valid on the falling edge of the signal line.
SHARED LINES (Open Collector)	IRQ1*-IRQ7* BR0*-BR4* SYSFAIL*	Hold X low Release X	Detect X low Detect X high (only if no drivers holding line low)	Indicates this line is activated in the low state.
(1) For other signal lines, see subparagraphs 1.4.3 and 1.4.8.				

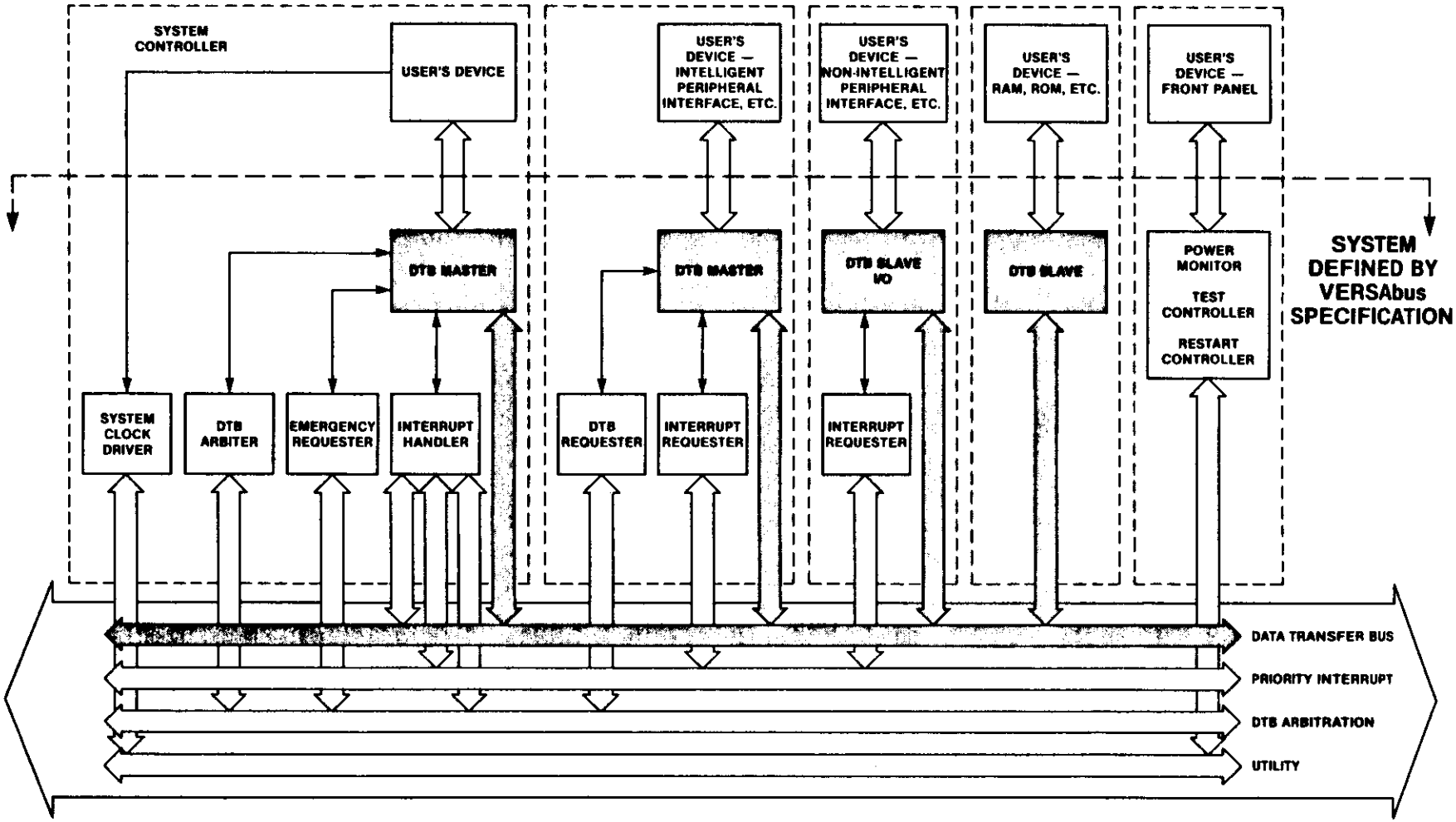
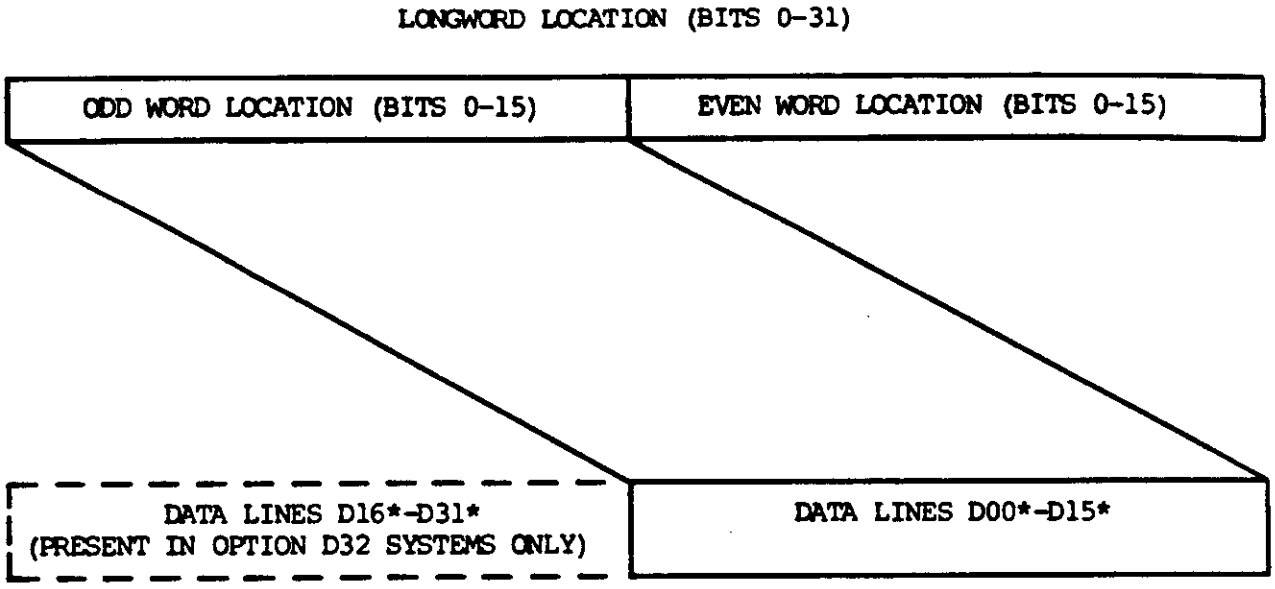
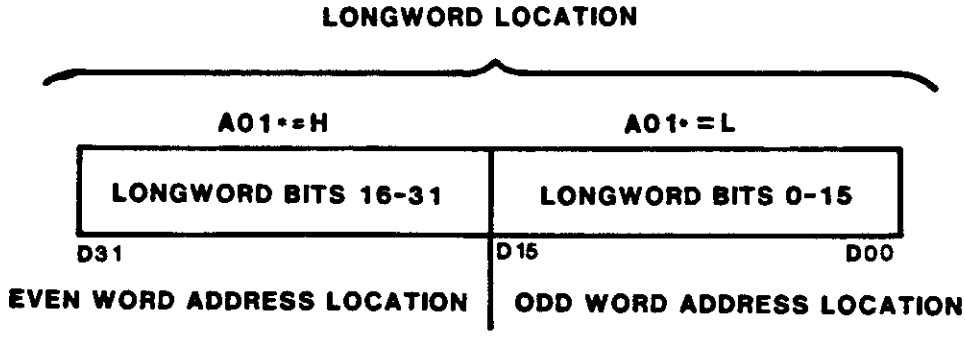


FIGURE 2-1. VERSAbus Data Transfer Functional Block Diagram



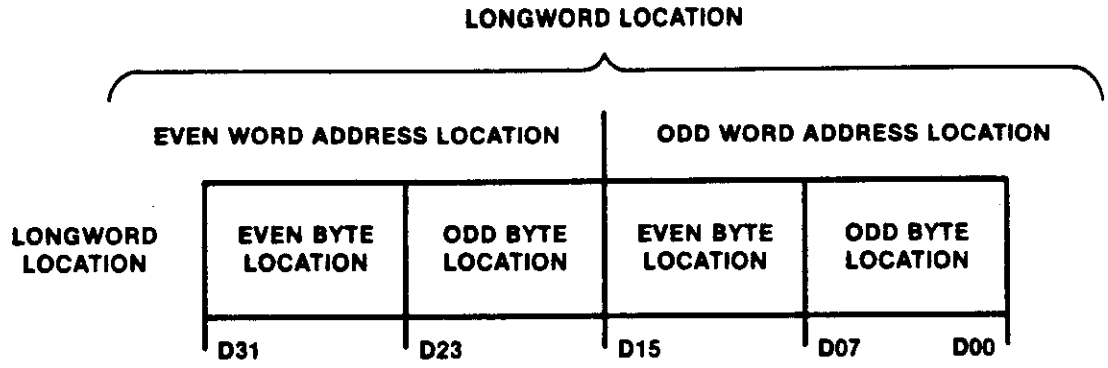
FOR A WORD ACCESS, THE DATA IS ALWAYS TRANSFERRED ON D00*-D15*.

FIGURE 2-4. Odd Word Location Accesses



THE ODD WORD LOCATION (A01 = 1) CORRESPONDS TO THE LONGWORD DATA BITS D00*-D15*.

FIGURE 2-5. Word Addressing of LONGWORD Locations



Byte Address	XX..X00	XX..X01	XX..XX10	XX..X11
Byte Access				
LWORD*	high	high	high	high
A01*	high	high	low	low
DS1*	low	high	low	high
DS0*	high	low	high	low
Word Access				
LWORD*	high	Note	high	Note
A01*	high	1	low	1
DS1*	low		low	
DS0*	low		low	
LONGWORD Access				
LWORD*	low	Note	Note	Notes
A01*	high	2	3	2 & 3
DS1*	low			
DS0*	low			

NOTES:

1. Not legal to access 16 bits of data on an odd byte address.
2. Not legal to access 32 bits of data on an odd byte address.
3. Not legal to access 32 bits of data on an odd word address.

FIGURE 2-6. Byte Location Numbering

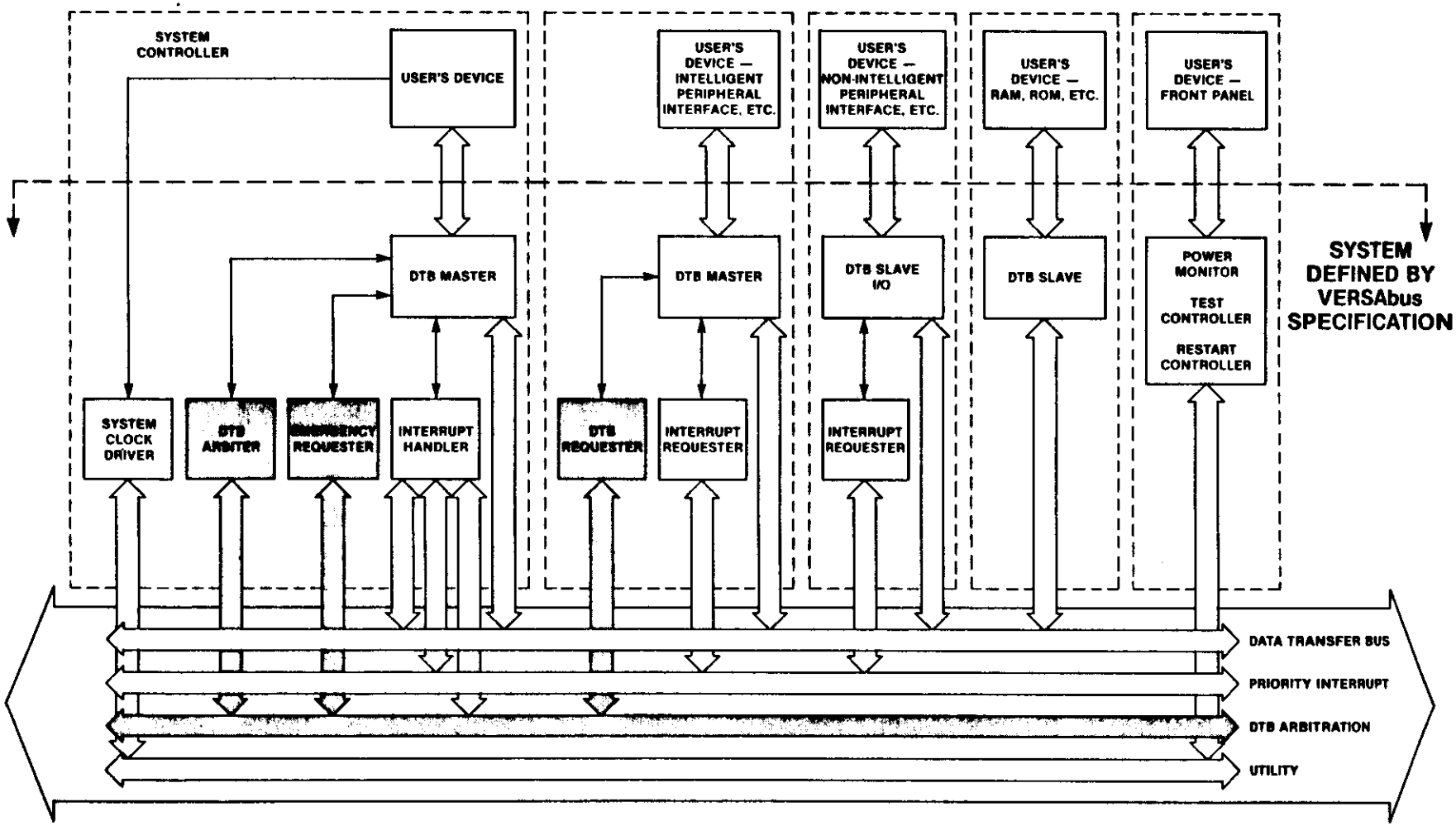


FIGURE 3-1. VERSAbus Arbitration Functional Block Diagram

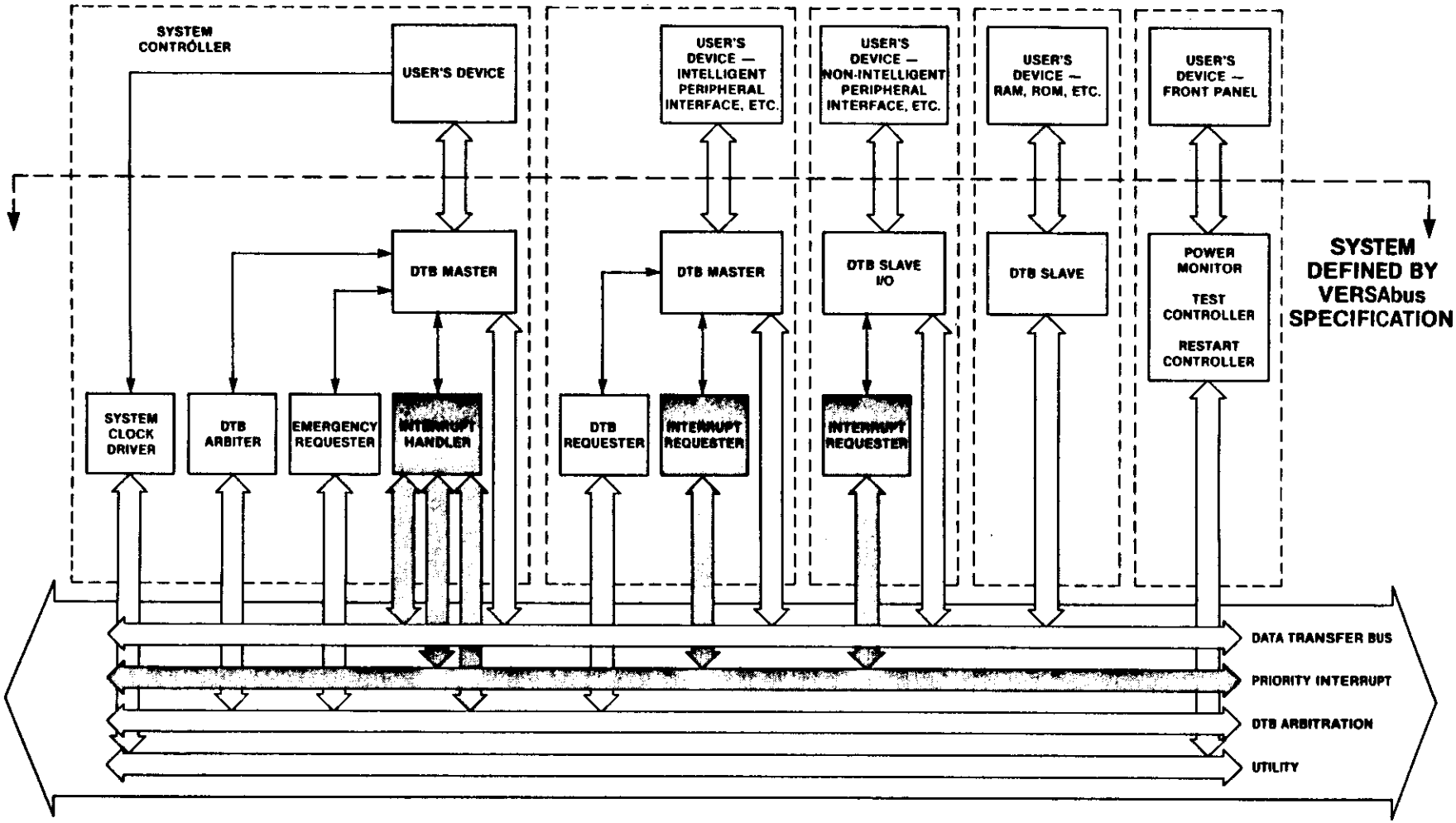


FIGURE 4-3. VERSAbus Priority Interrupt Functional Block Diagram

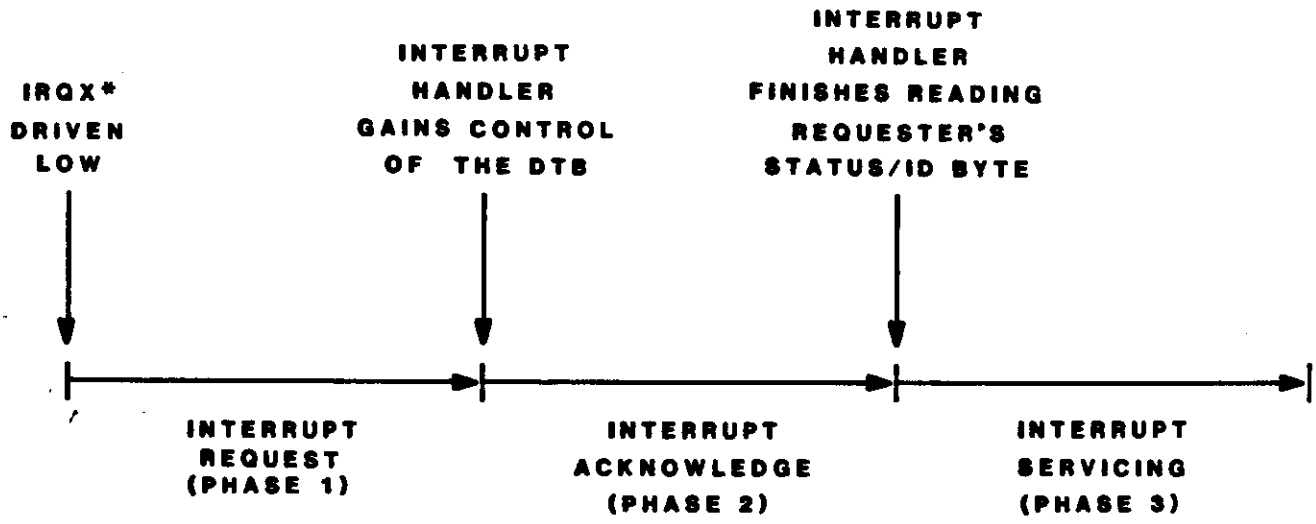


FIGURE 4-6. The Three Phases of an Interrupt Sequence

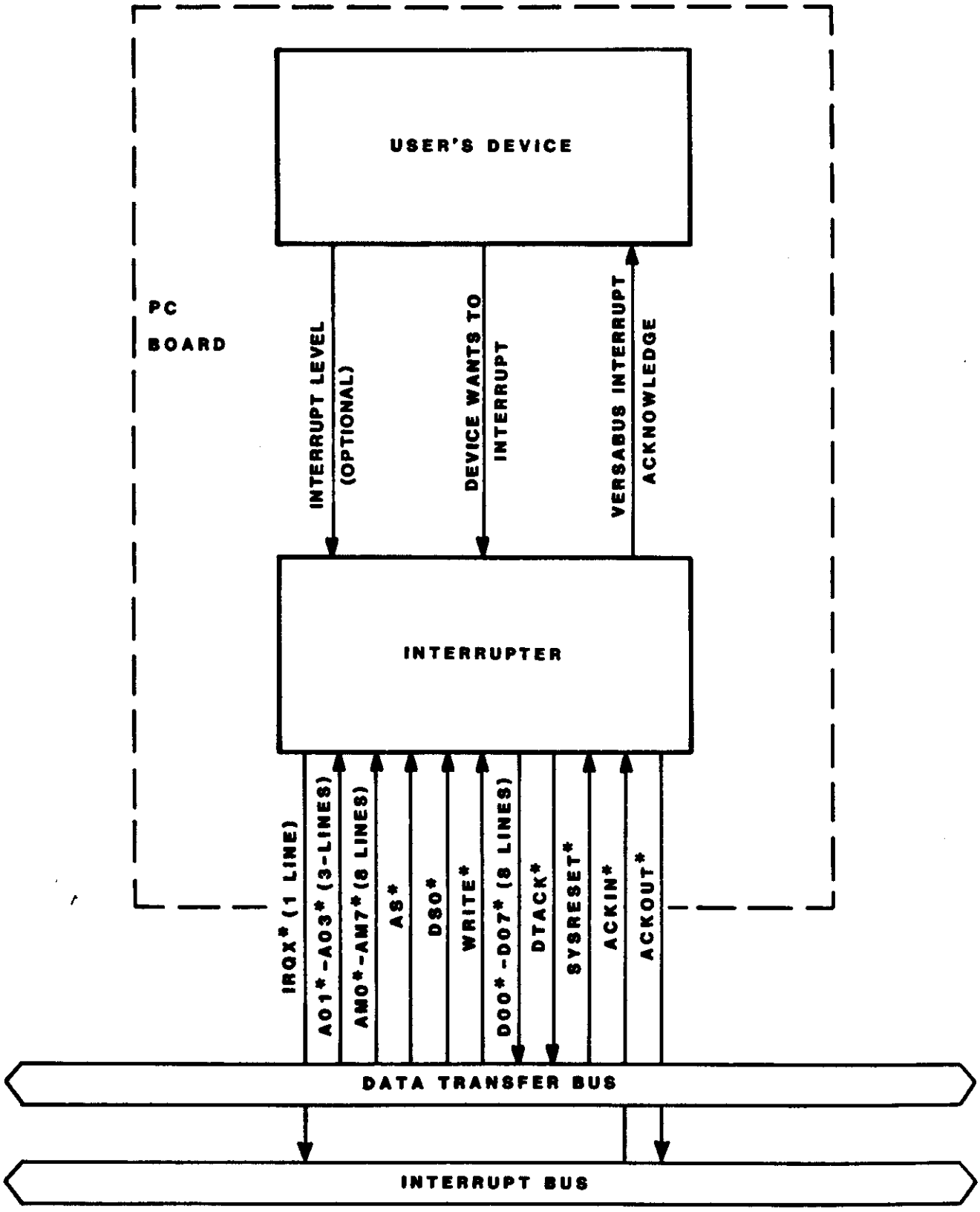


FIGURE 4-13. INTERRUPTER Block Diagram

4.5.2 INTERRUPT HANDLER

Figure 4-14 shows the block diagram of an INTERRUPT HANDLER. The INTERRUPT HANDLER consists of three sub-elements:

a. Interrupt prioritizer

b. Address bus driver

c. Data bus controller

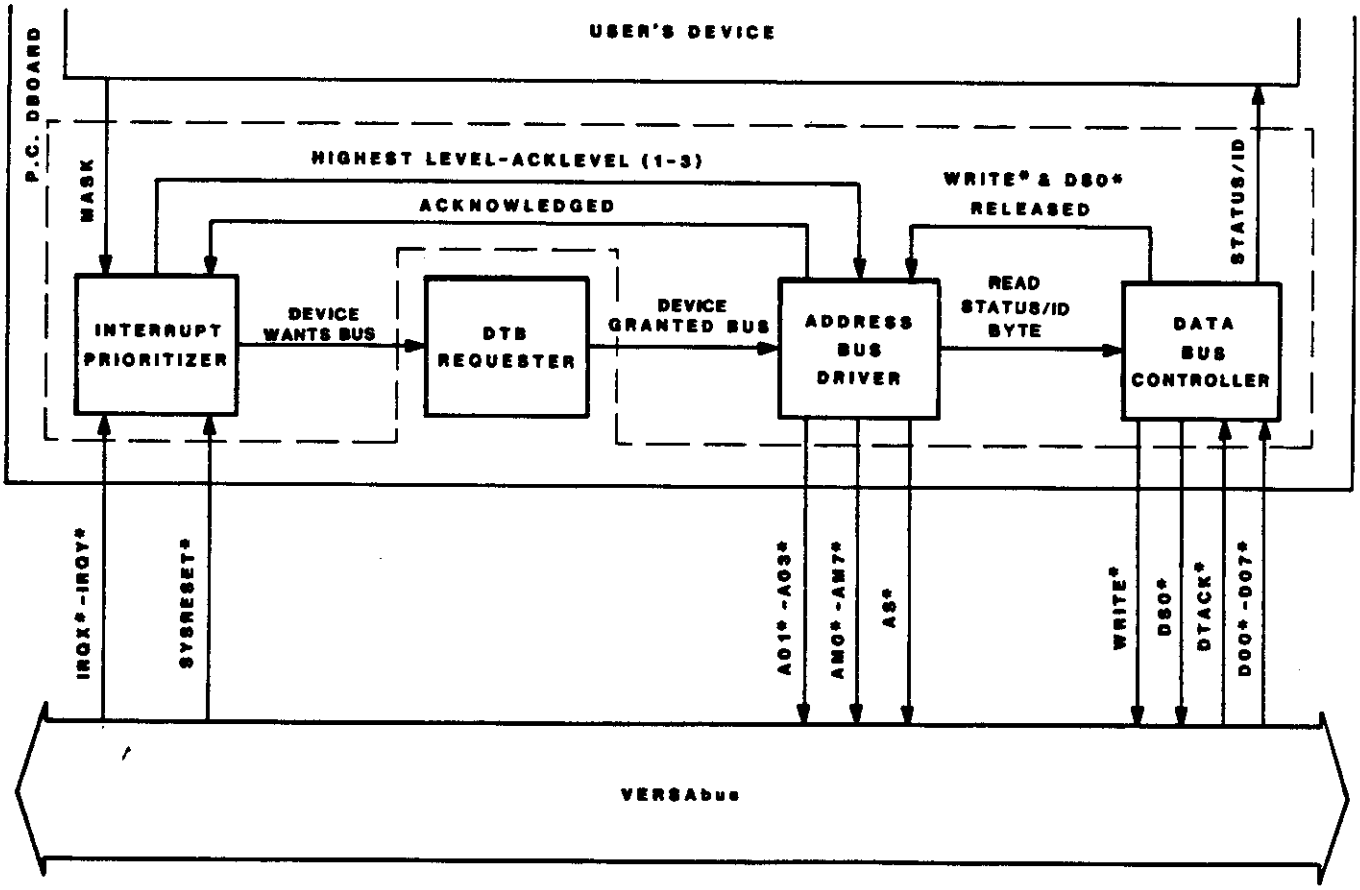
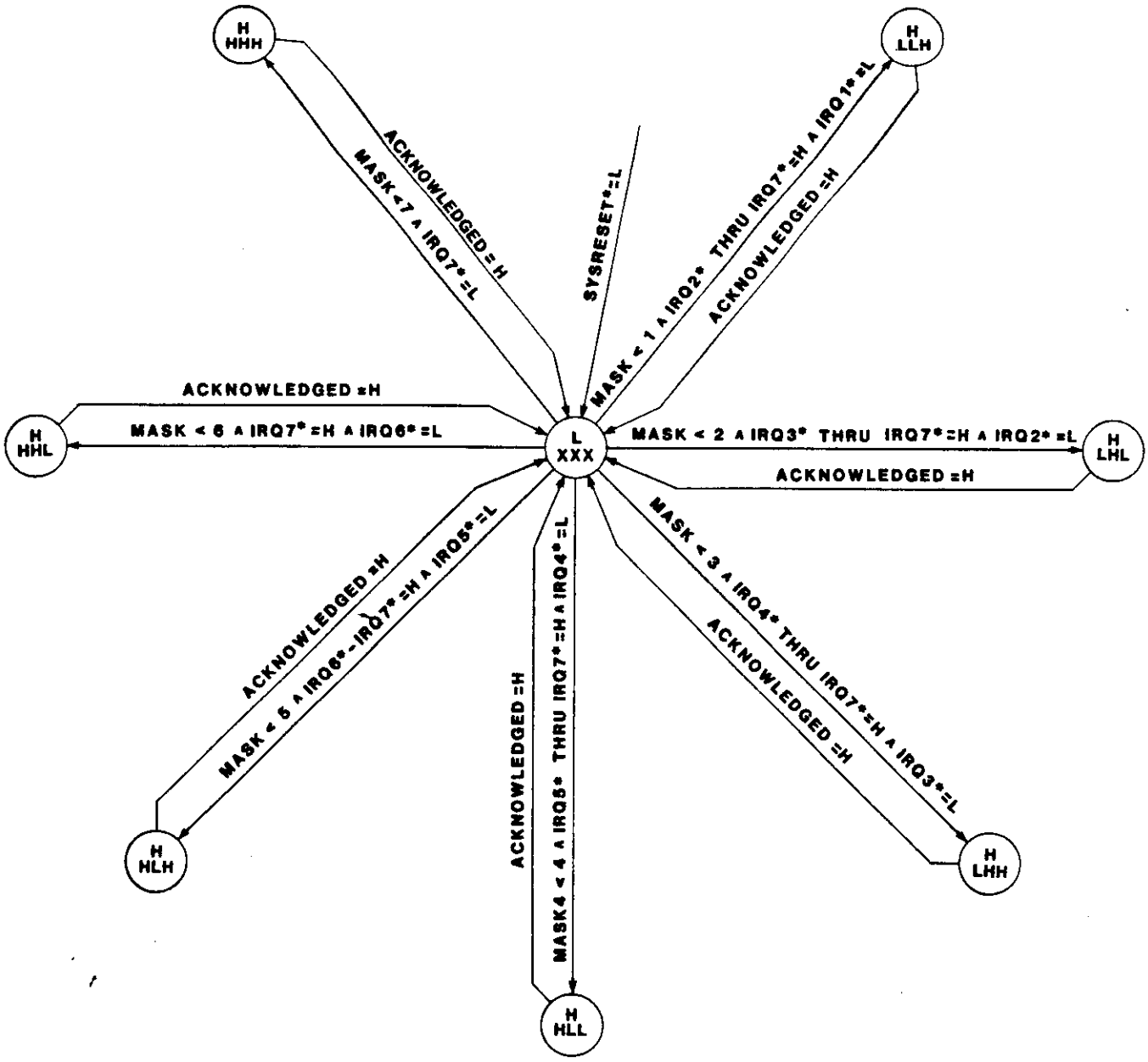


FIGURE 4-14. Block Diagram: INTERRUPT HANDLER



THE STATES ON THIS DIAGRAM ARE LABELLED ACCORDING TO THE LEVELS OF THE INTERRUPT PRIORITIZERS OUTPUT LINES.

DEVICE WANTS BUS		
ACK LEVEL 3	ACK LEVEL 2	ACK LEVEL 1

FIGURE 4-15. State Diagram for the Interrupt Prioritizer of a Seven Level INTERRUPT HANDLER

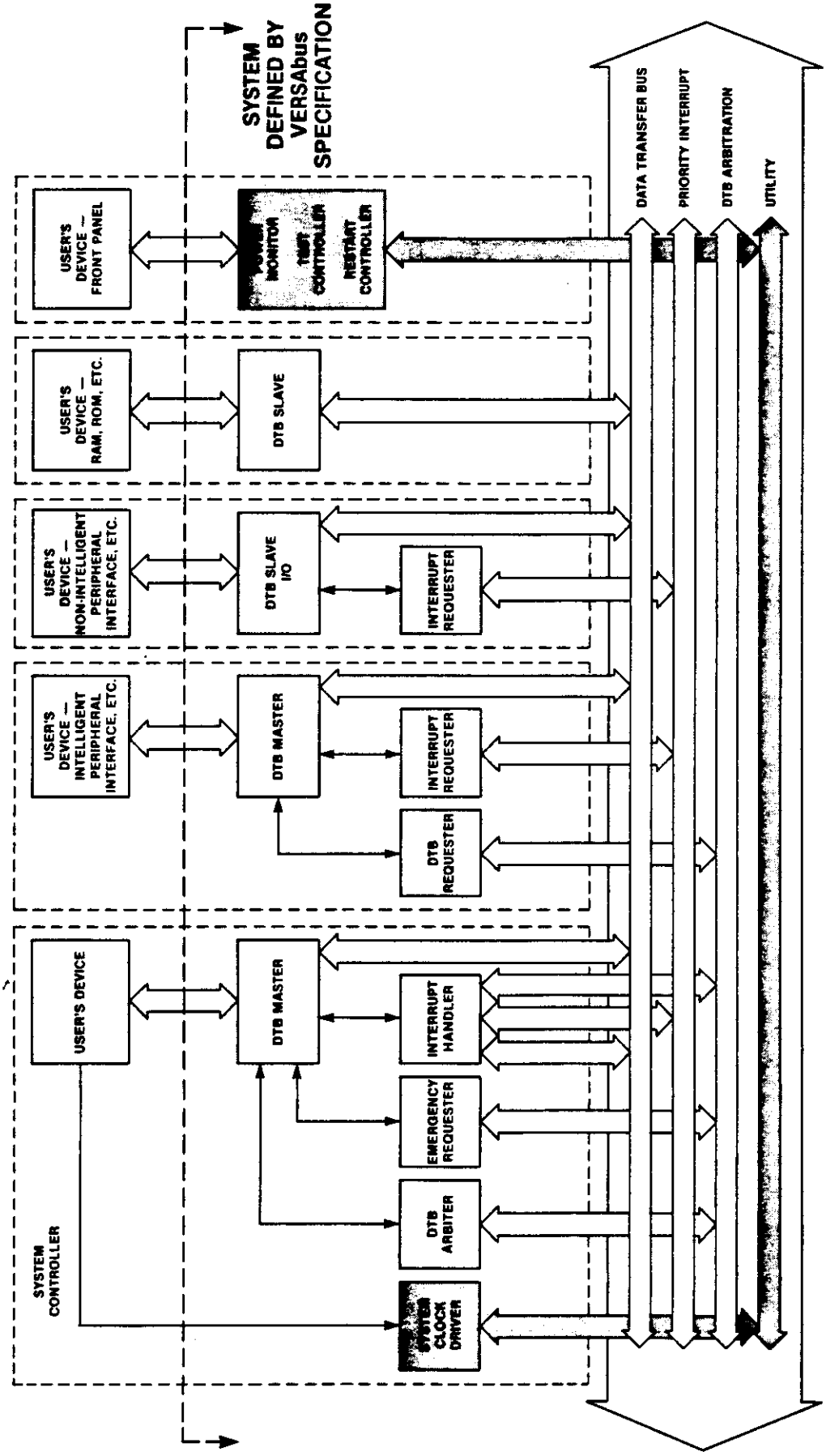


FIGURE 5-1. VERSAbus Utility Block Diagram

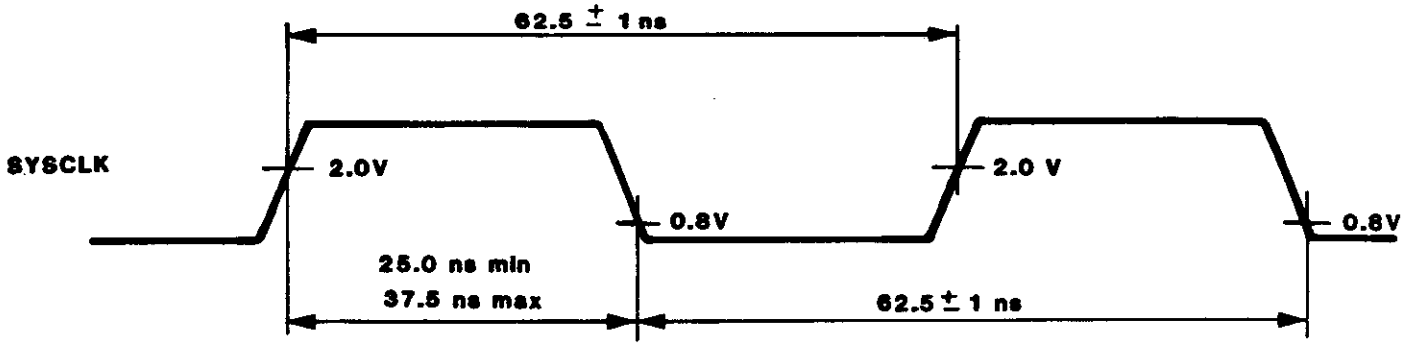


FIGURE 5-2. System Clock Timing Diagram

5.2.1.2 AC Clock (ACCLK) Specification

The AC clock is a 50 or 60 hertz (nominal) signal derived from the power supply line frequency. It can be used as a clock source to generate time-of-day, or to detect line frequency zero-point crossings. Figure 5-3 illustrates the timing relationship between the edges of ACCLK and the zero crossings of the AC line. ACCLK edges may lead or lag the AC zero crossing by a maximum of 115 usecs on a 50 cycle system, or 95 usecs on a 60 cycle system.

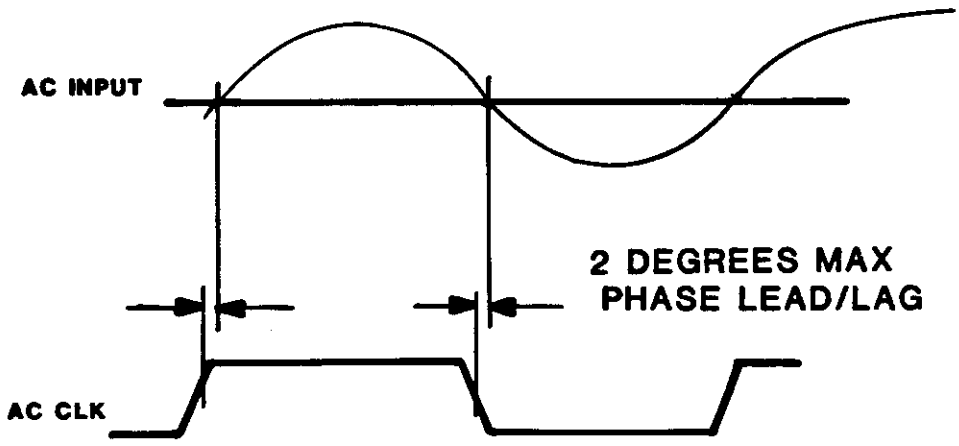


FIGURE 5-3. AC Clock Timing Diagram

5.3 POWER MONITOR MODULE

This module is usually an external PC board (Figure 5-5) upon which the ACFAIL*, ACCLK, and (optionally) TEST0*, TEST1*, and SYSRESET* drivers are located. Logic to interface an operator's panel and to detect power fail may also be placed on this circuit card.

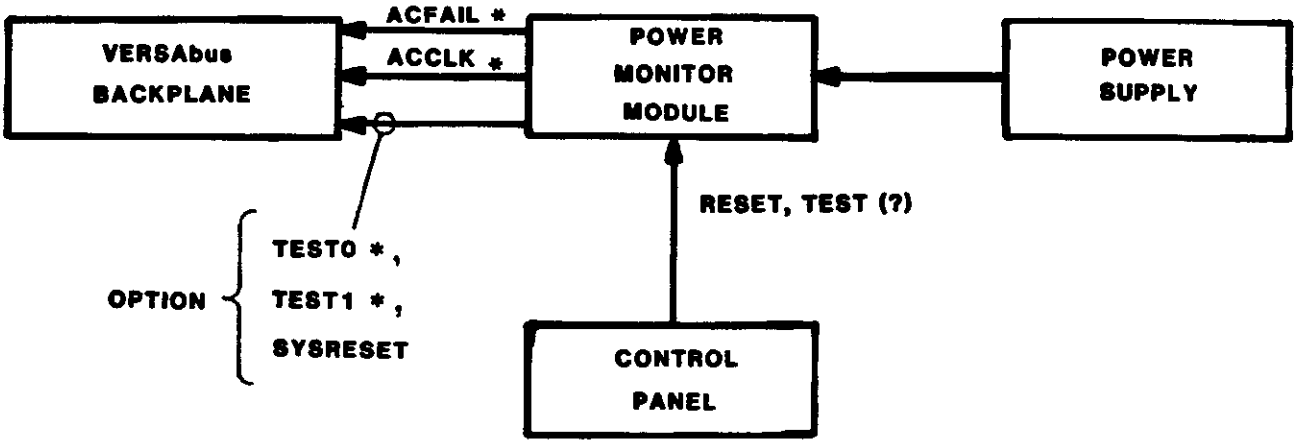


FIGURE 5-5. Block Diagram of POWER MONITOR Module

The ACFAIL* and SYSRESET* signals and the point at which the system DC voltages violate specification have certain timing constraints. These constraints are spelled out in Figures 5-6 and 5-7.

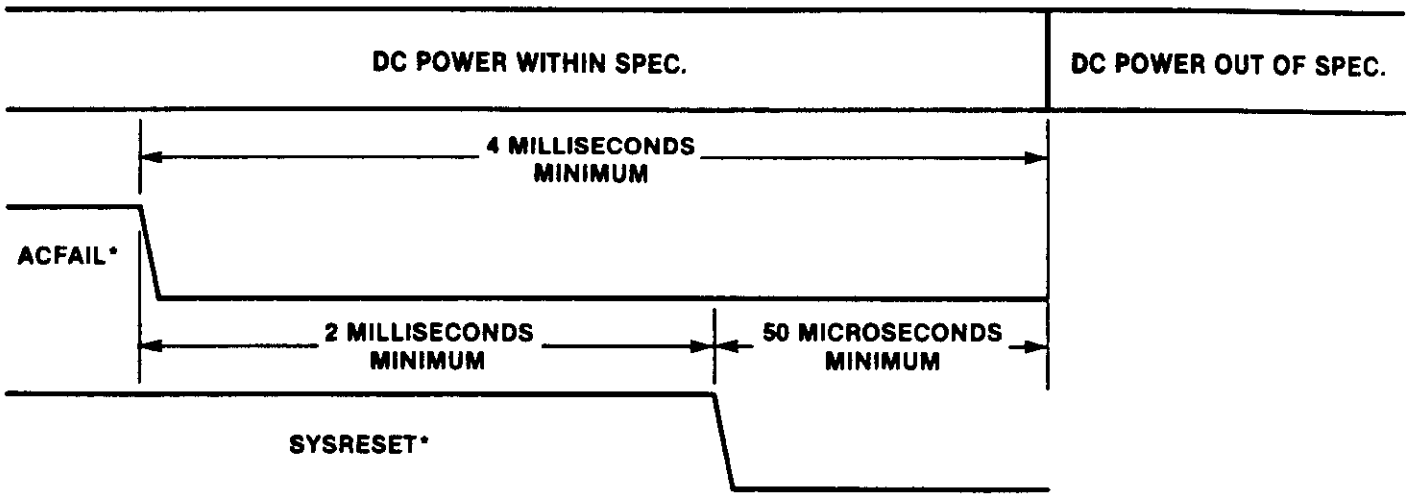


FIGURE 5-6. System Power Fail Timing

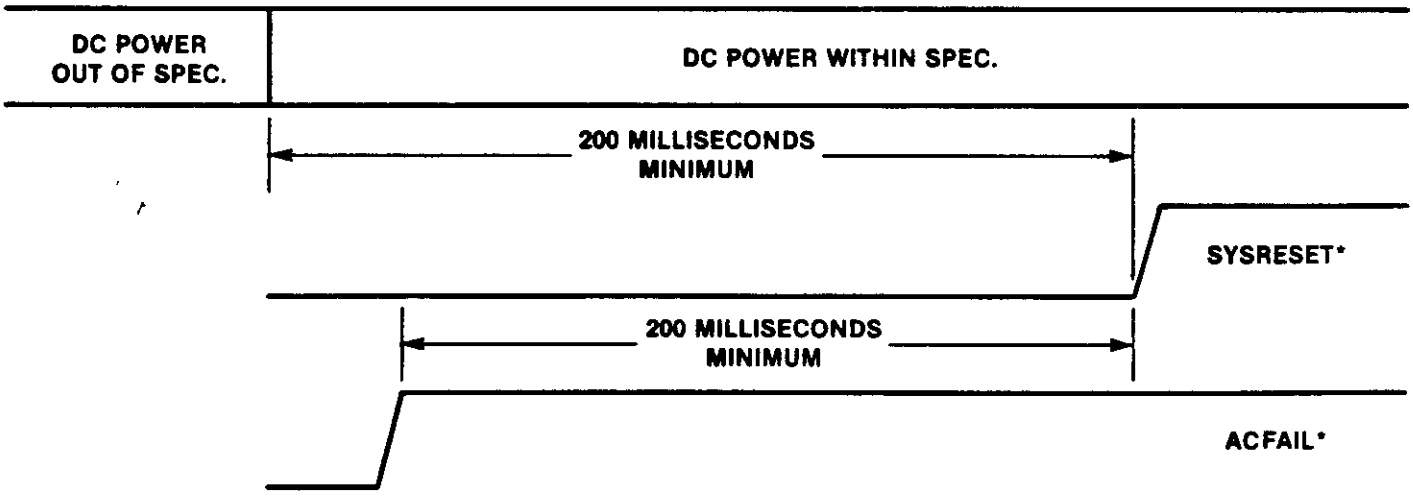


FIGURE 5-7. System Power Restart Timing

TABLE 7-1. Bus Voltage Specifications

MNEMONIC	DESCRIPTION	VARIATION (see NOTE)	RIPPLE & NOISE BELOW 10 MHz (PK-PK)	CONNECTOR P1 PIN NUMBER	CONNECTOR P2 PIN NUMBER	MAXIMUM CURRENT DRAW PER SLOT
+5V	+5 Vdc power	+5.0%/-2.5%	50 mV	1,2,129-132	7 - 10	8 amps
+12V	+12 Vdc power	+5.0%/-3.0%	50 mV	125 - 128	11 - 12	6 amps
-12V	-12 Vdc power	+3.0%/-5.0%	50 mV	121 - 122	15 - 16	3 amps
+5V STDBY	+5 Vdc standby	+5.0%/-2.5%	50 mV	133 - 134	-	3 amps
+15V	analog power	+5.0%/-3.0%	25 mV	-	69 - 70	3 amps
-15V	analog power	+3.0%/-5.0%	25 mV	-	67 - 68	3 amps
GND	ground	Ref.	Ref.	3,4,23-24, 27-28,31-32, 61-62,67-68, 71-72,119-120, 123-124,139-140	1-2,3-4,5-6, 97-98,101-102	
15V GND	$\pm$15V ground return	Ref.	Ref.	-	13 - 14	

NOTE: The non-symetric variation spec is given to ensure that the DC power will remain within the $\pm$5% tolerance required by most IC's despite any drops resulting from power distribution on individual VERSAboards.

7.3 ELECTRICAL SIGNAL CHARACTERISTICS

Other than power supply lines, all VERSAbus signals are limited to positive levels between 0 and 5.0 volts. As described in paragraph 1.4.1, the signal levels are:

a. 0.0 V $\leq$ Low level $\leq$ 0.8 V
b. 2.0 V $\leq$ High level $\leq$ 5.0 V

Figure 7-1 gives a simple graphic representation of these levels.

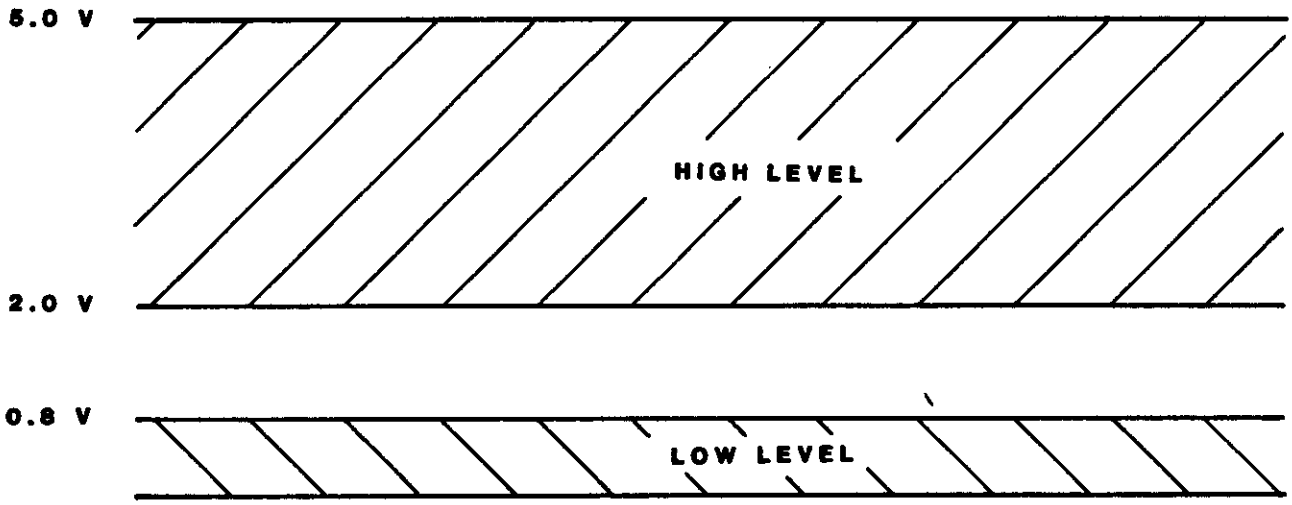


FIGURE 7-1. VERSAbus Signal Levels

Depending on the function required, VERSAbus uses three-state, wired-OR, and totem pole drivers. The drivers are specified in paragraph 7.4, and the receivers are specified in paragraph 7.5. Appendix C lists signal lines by function, and gives their associated characteristics.

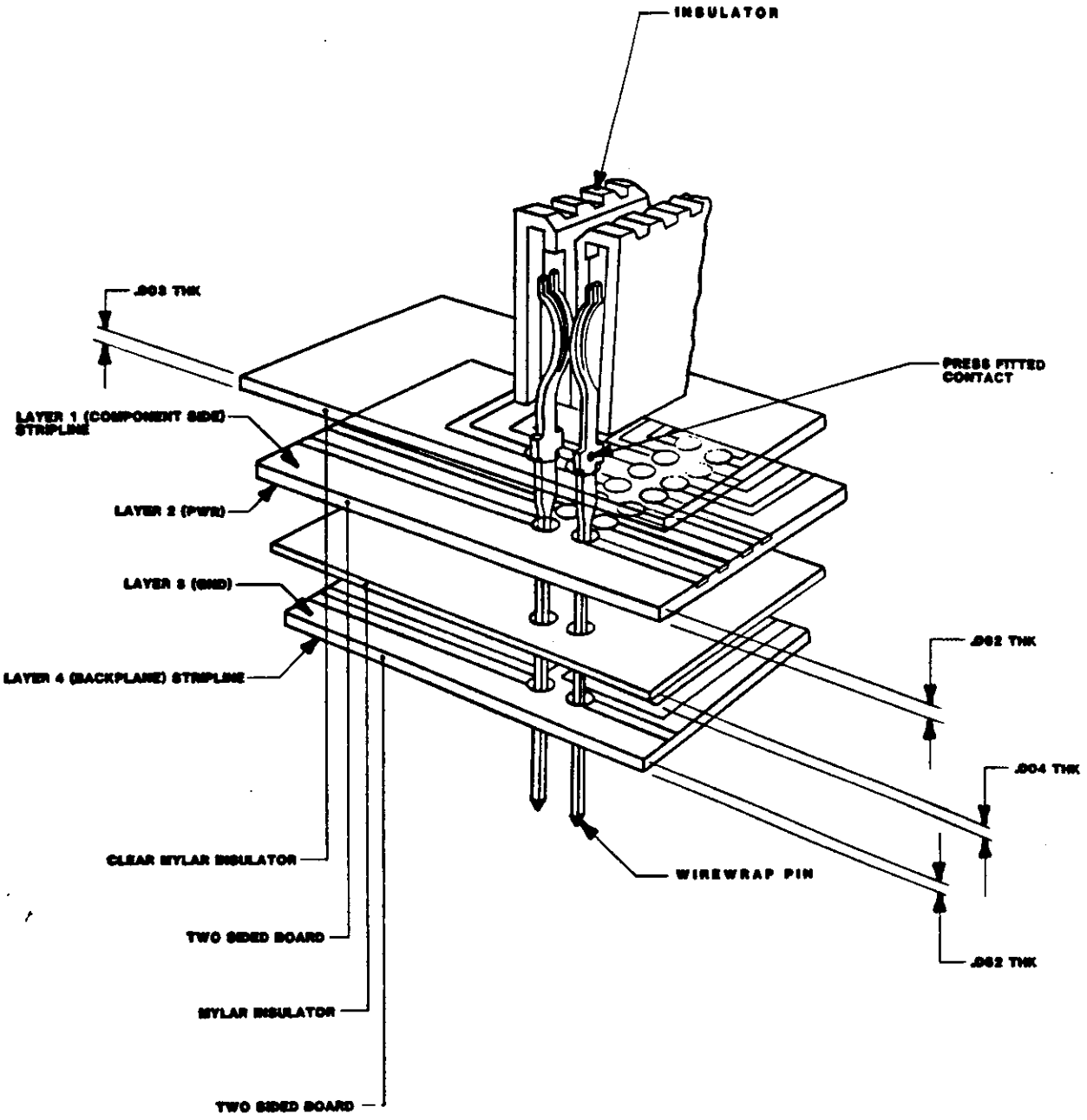


FIGURE 8-1. Typical Multilayer Backplane/PCB Construction Technique

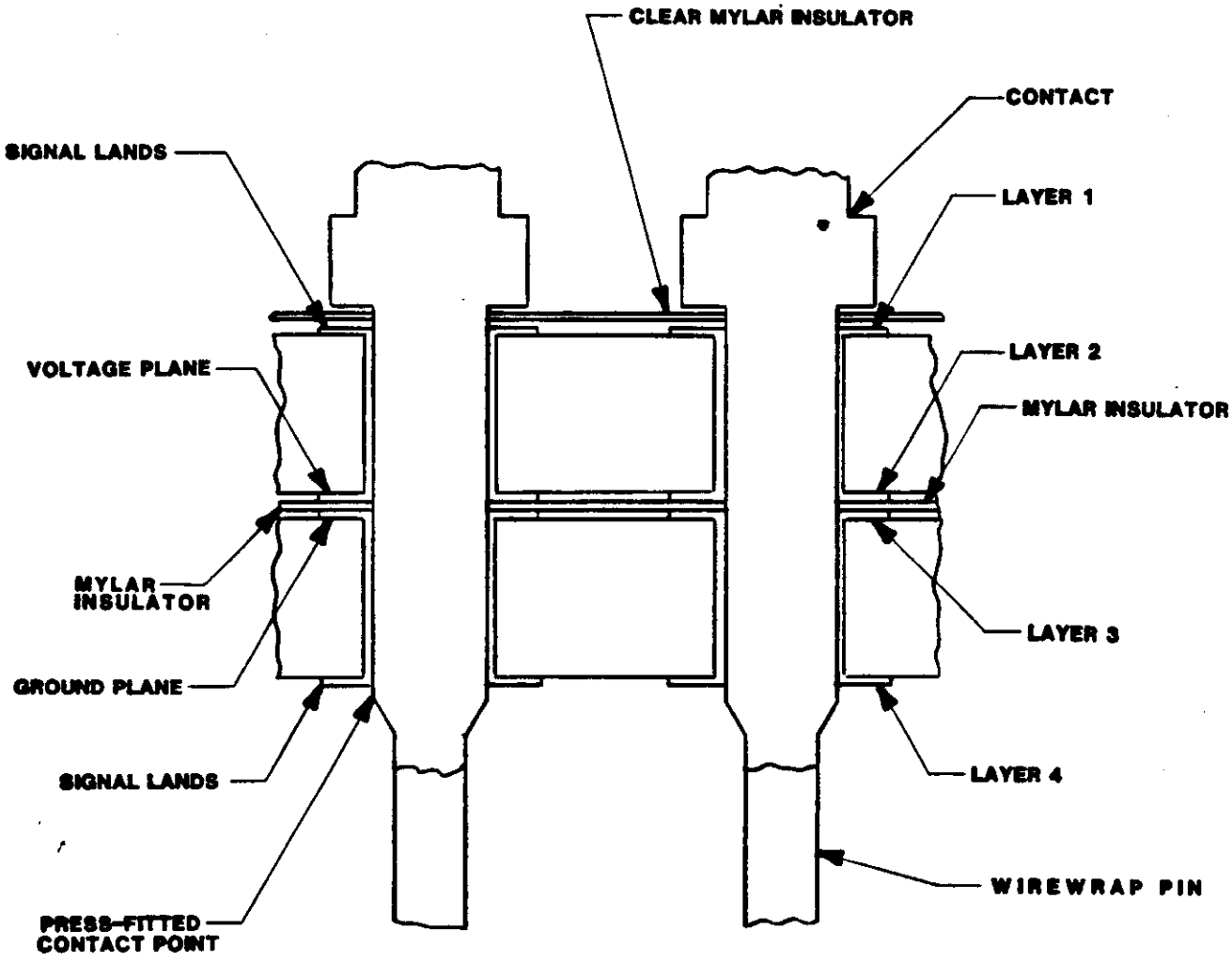


FIGURE 8-2. Typical Multilayer Backplane/PCB Cross-Sectional Area View

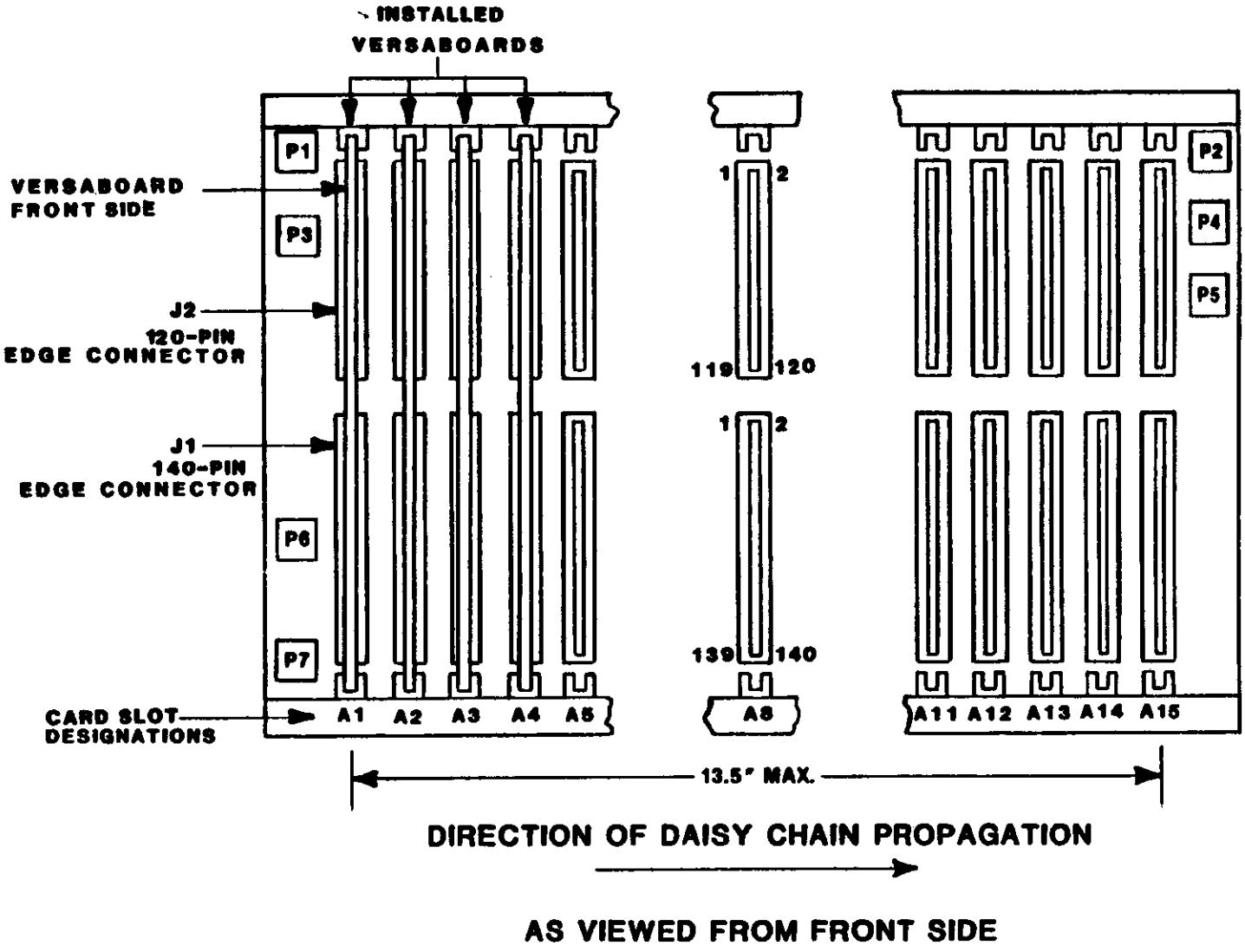


FIGURE 8-3. Backplane Reference Designations and Pin Numbering Standard

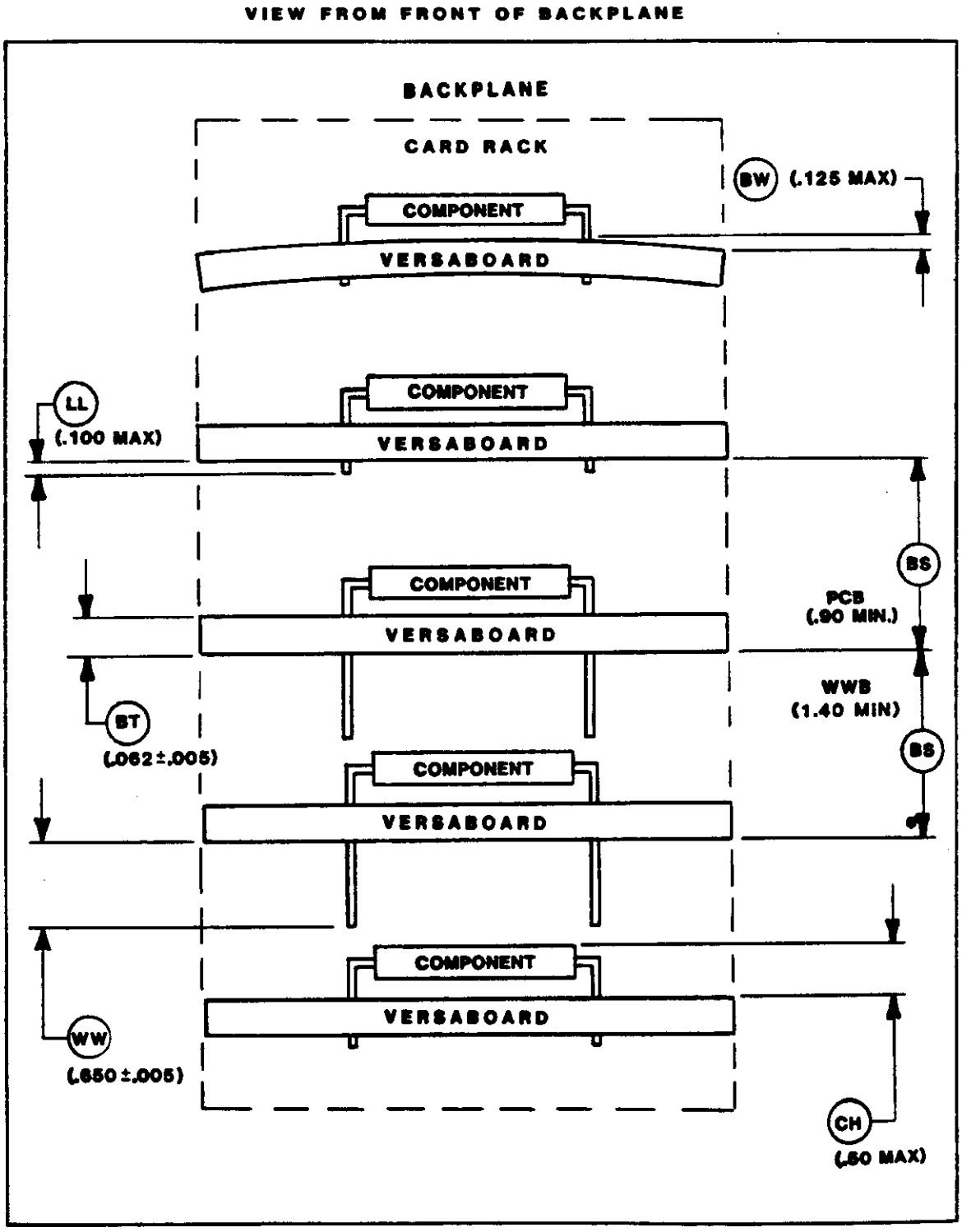
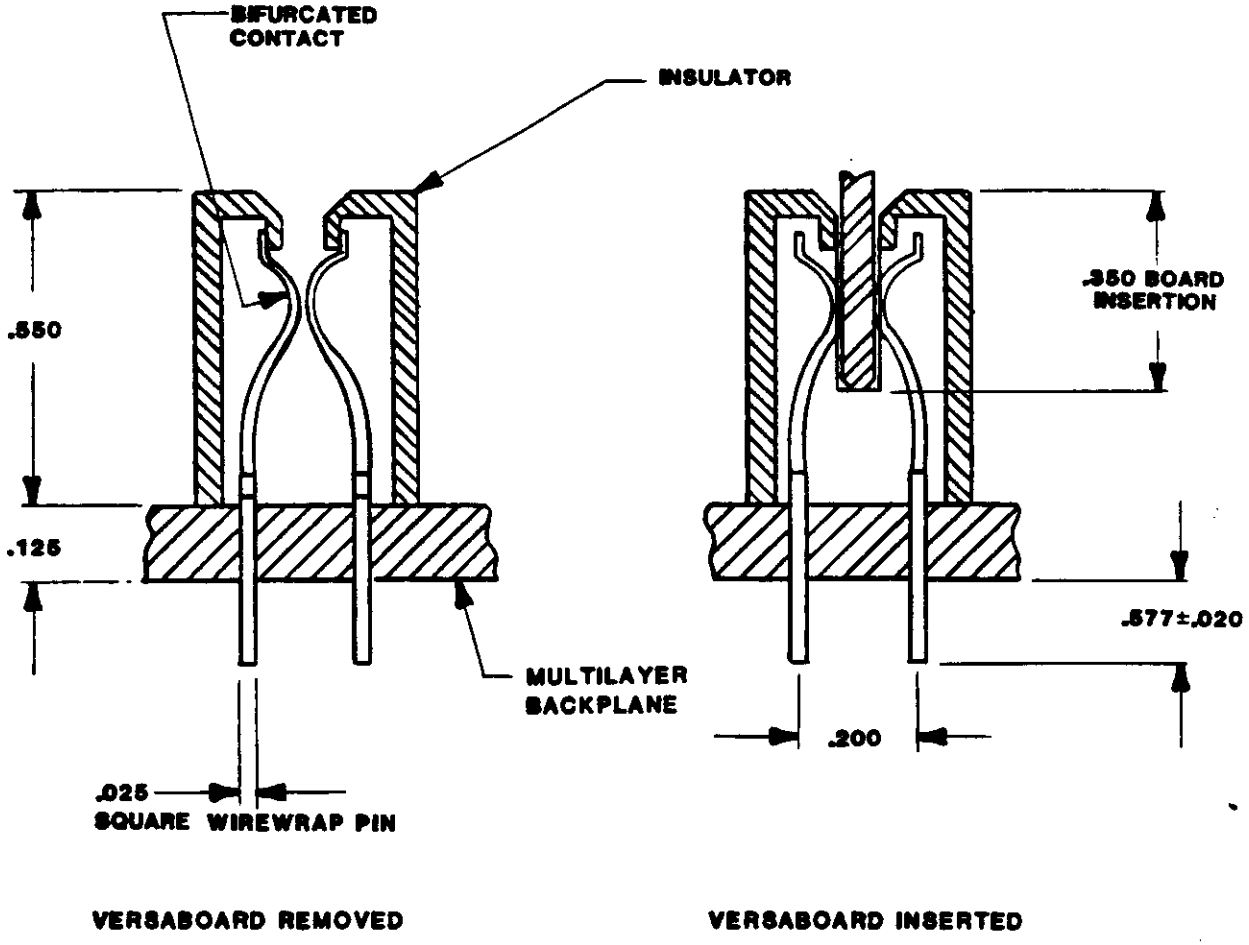


FIGURE 8-4. Backplane/VERSAboard Dimensional Requirements



CAUTION

THE ABOVE DIMENSIONS CAN VARY, DEPENDING ON MANUFACTURER.

FIGURE 8-5. Typical Backplane Edge Connector

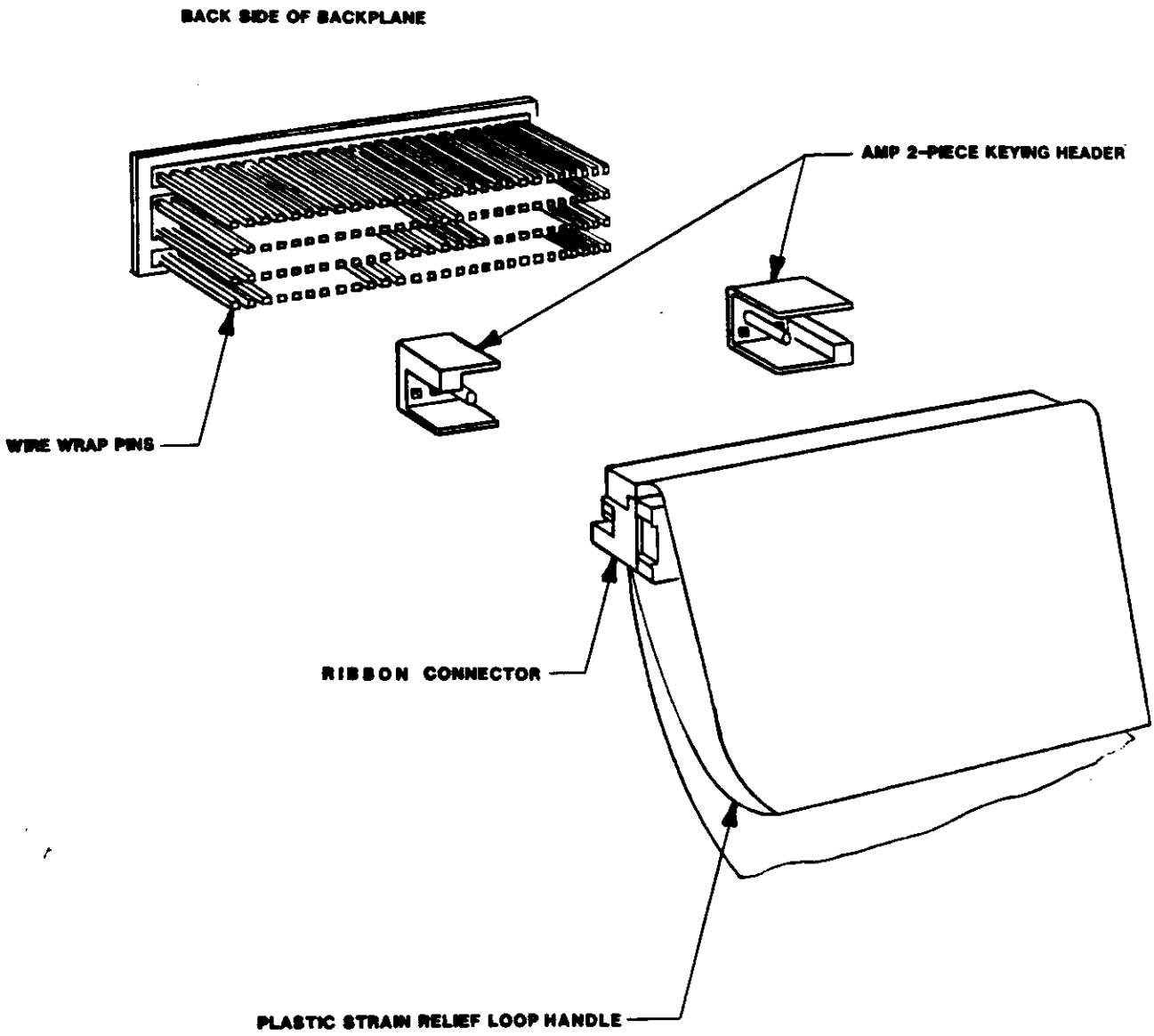


FIGURE 8-6. I/O Cable Connection

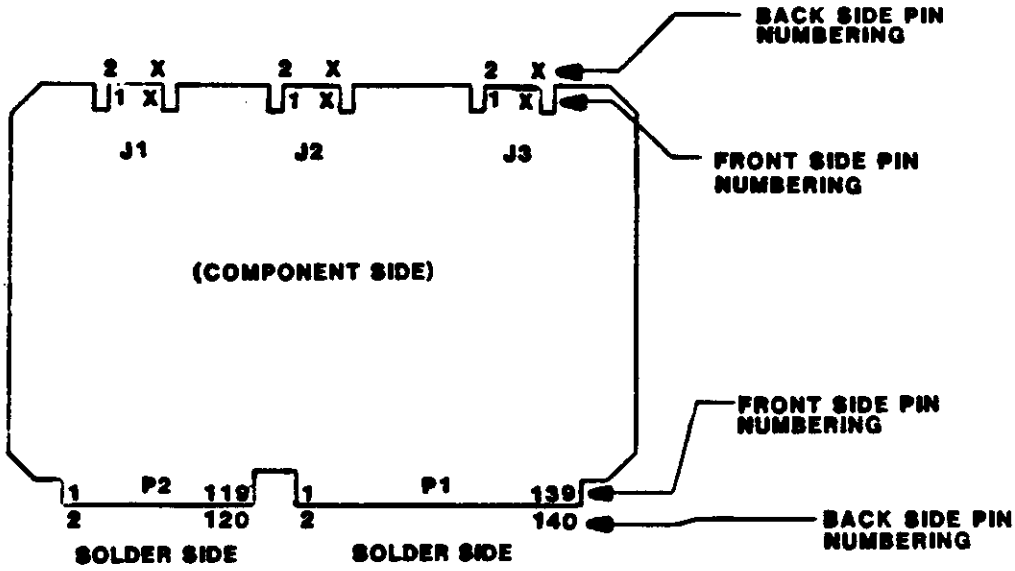


FIGURE 8-10. VERSAboard Reference Designations and Pin Numbering Standards

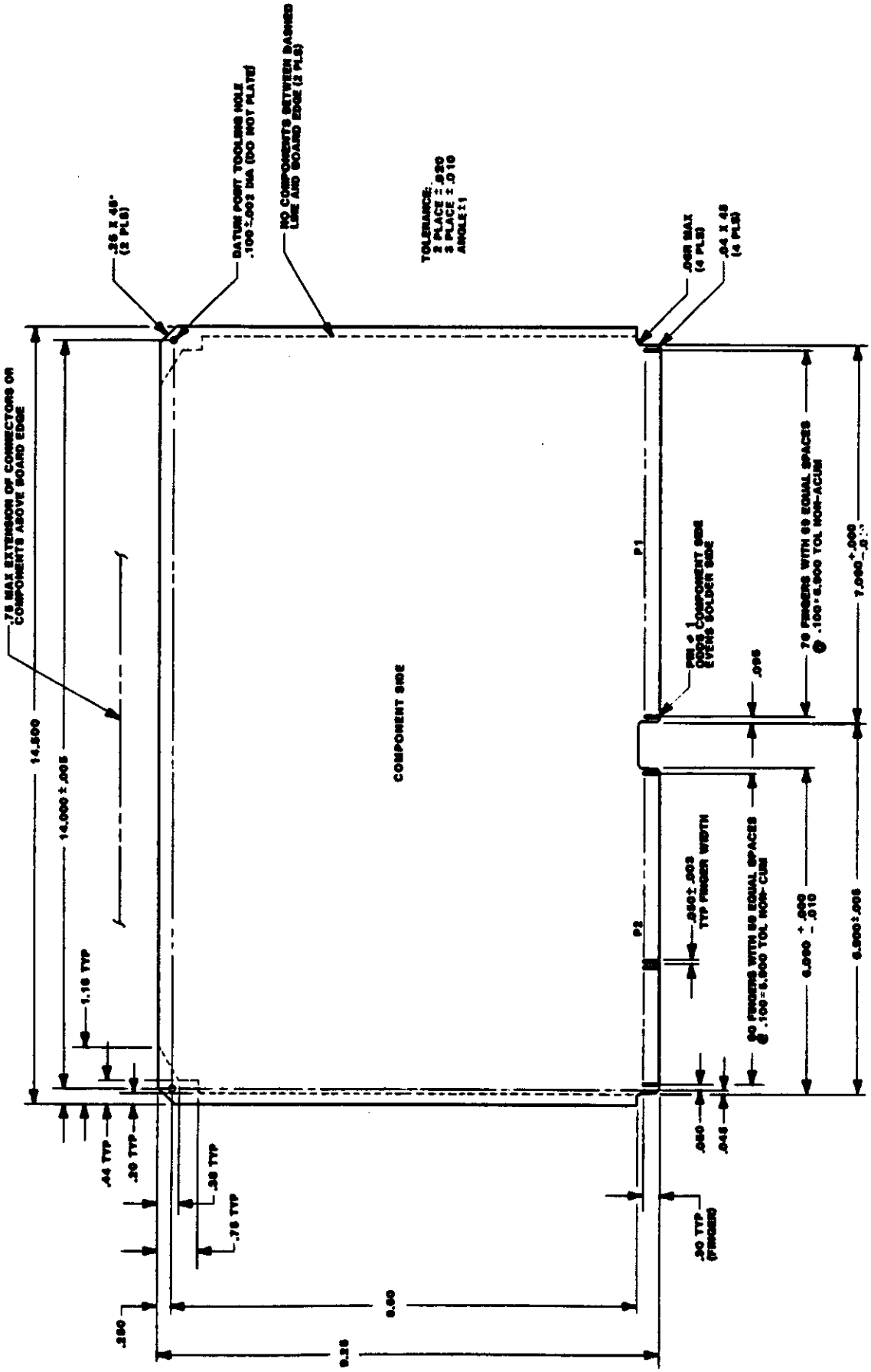


FIGURE 8-11. Standard Size PCB

APPENDIX A

GLOSSARY OF VERSAbus TERMS

Axx* - the symbolic notation for a particular address line on the VERSAbus, where 'xx' may have the values 01 through 31. These lines are driven by the module currently designated as the VERSAbus MASTER to selectively address one and only one other module. The module is designated as the addressed SLAVE for the purpose of initiating a data transfer between two modules.

A24 - the VERSAbus option which identifies a particular module as capable of driving or responding to only 23 address lines. (See the section on SUBSET compatibility for further information.)

A32 - the VERSAbus option which identifies a particular module as capable of driving or responding to all 31 address lines. (See the section on SUBSET compatibility for further information.)

APARITY0* - the parity line associated with the signal lines A01* through A23*, LWORD*, and AM0* through AM7*. This line represents the 'exclusive OR' of the 32 lines above. Therefore, the 'exclusive OR' of this line with all of those lines should always be zero. This condition is often referred to as even parity. If the MASTER currently in control of the VERSAbus and the SLAVE being addressed are both option AP (meaning: address parity), then the MASTER will generate this parity signal and the SLAVE will verify it. (See the section on SUBSET compatibility for further information on other combinations of MASTER and SLAVE options.)

APARITY1* - the parity line associated with the signal lines A24* through A31*. This line represents the exclusive OR of these eight additional address lines used in extended addressing on the VERSAbus, Option A32. (See APARITY0* for additional details and the section on SUBSET compatibility for information on combinations of MASTER and SLAVE options.)

AP - the option designated when a module will properly generate (if MASTER) or test (if SLAVE) address parity.

APVAL* - a signal line driven low by AP MASTERS whenever they place an address on VERSAbus. This low level indicates to the addressed SLAVE that the APARITY lines are valid. If the SLAVE is option AP, it will verify this parity.

ARBITER - the term used to reference the logic circuitry connected to VERSAbus at slot 1 to perform the task defined as ARBITRATION. (See ARBITRATION for additional definition. See the chapter on bus arbitration for detailed description.)

ARBITRATION - the task of assigning control of the data transfer bus on a priority basis to a requester. (For detailed material, see the chapter on bus arbitration.)

AS* - the address strobe line of the VERSAbus. When a MASTER has assumed control of the bus and has driven this line low, it is a signal to all SLAVES that the address bus is now valid and that a data transfer is initiated. The last act of a given MASTER in a data transfer cycle must be to release this line to the TRI-STATE condition, so that all units may know that this data transfer is over and that, if the 'bus busy' line is also released, the DTB is now available to be reassigned to the next MASTER. For detailed information on timing considerations, see the timing section of the Data Transfer Bus chapter.

BGxIN*/BGxOUT* - the symbolic notation used for a particular bus grant line on the VERSAbus, where 'x' may have the values 0 through 4. These lines are used to grant a particular level of data transfer bus access from the bus ARBITER, and represent a set of lines on the bus which are not bused, but daisy-chains. In particular, this nomenclature refers to the signal being forwarded to the next module in the chain. If this module does not use the particular level in question, the path from BGxIN* to BGxOUT* will probably be a jumper; but if this board uses the level, the signal will be passed through an AND gate, so that if the board receives the signal, and has a request pending, it may inhibit the signal from continuing down the bus and triggering activity on two MASTERS simultaneously. Not only does this methodology provide a means for having more MASTERS than levels of bus request, but it provides a secondary level of prioritization within a given level of bus request, which is physically determined by proximity to slot 1. (See also the chapter on bus arbitration.)

BRx* - the symbolic notation used for a particular bus request line on the VERSAbus, where 'x' may have the values 0 through 4. These lines are used to request control of data transfer bus access from the bus ARBITER.

Dxx* - the symbolic notation for a particular data line on the VERSAbus, where 'xx' may have the values 00 through 31. These lines are used by one module to selectively transfer data to one and only one other module.

DTB - an acronym for DATA TRANSFER BUS. This is the particular subset of VERSAbus lines involved in a data transfer, consisting of the address lines, the address parity lines, the data lines, the data parity lines, and the lines LWORD*, WRITE*, AS*, DS0*, DS1*, DTACK*, and BERR*.

DPARITY0* - the parity line associated with the signal lines D00* through D07*. This line represents the 'exclusive OR' of those eight data lines. Therefore, the 'exclusive OR' of this line with all of those lines should always be zero. This condition is often referred to as even parity. If the module currently providing data to the VERSAbus is defined as having option DP, it will generate this signal. If the module currently receiving the data is defined as having option DP, it will verify this parity and flag errors. (See the section on SUBSET compatibility for further information on various combinations of options.)

DPARITY1* - the parity line associated with the signal lines D08* through D15*. This line represents the 'exclusive OR' of eight of the data lines referenced by DS1*. (See DPARITY0* for more details.)

DPARITY2* - the parity line associated with the signal lines D16* through D23*. This line represents the 'exclusive OR' of eight of the data lines used during longword transfers, and is only driven by modules having option D32. (See DPARITY0* for more details on parity, and the section on SUBSET compatibility for further information on various combinations of options.)

DPARITY3* - the parity line associated with the signal lines D24* through D31*. This line represents the 'exclusive OR' of eight of the data lines used during longword transfers, and can only exist on modules having option D32. (See DPARITY0* for more details on parity, and the section on SUBSET compatibility for further information on various combinations of options.)

DPVAL* - a signal line driven low by DP MASTERS and DP SLAVES whenever they place data on VERSAbus. This low level indicates to the MASTER/SLAVE receiving the data that the DPARITY lines are valid and may be used to verify data.

DP - the option designated when a module will generate data parity when presenting data, and test data parity when receiving data.

LONGWORD - a data transfer operation involving 32 bits of transferred data, which is invoked by a MASTER module driving the signal LWORD* to the low state. Note that only modules classified as having option D32 can be expected to transfer long words. (See the section on SUBSET compatibility for further material.)

LWORD* - the signal on the VERSAbus used to invoke 32-bit data transfers (See also LONGWORD.)

MASTER - a module capable of requesting control of the VERSAbus data transfer bus via its associated REQUESTER, and upon being signaled by its REQUESTER that the data transfer bus has been granted, is capable of addressing another module by driving the address lines and sending data to or receiving data from the module so addressed.

NAP - the option designated when a module will not generate (if MASTER) or test (if SLAVE) address parity.

NDP - the option designated when a module will not generate or test data parity.

NPF - the option designated for a VERSAbus ARBITER which does not have the additional logic on board to allow response to a system MASTER under emergency conditions such as power down. (See chapter on bus arbitration and definition of PF for further details.)

PF - the option designated for a VERSAbus ARBITER capable of responding to the BREL* signal as an emergency bus request. (See chapter on bus arbitration for further details.)

READ - a data transfer initiated by a MASTER, with the data flow from MASTER to SLAVE.

SLAVE - a module capable of decoding the address lines of the VERSAbus, and properly responding to a MASTER by accepting or rejecting data transfers via the DTACK* and BERR* response lines when the address presented matches one recognized by this SLAVE as within its range.

System MASTER - a designation for that MASTER which has the responsibility for saving and restoring data at system power up, system power down, and other emergency handling. Through the use of a PF ARBITER, the system MASTER can gain quick control of the data transfer bus for emergency purposes.

WRITE - a data transfer initiated by a MASTER, with the data flow from MASTER to SLAVE.

APPENDIX C

VERSAbus CONNECTOR/PIN DESCRIPTION

INTRODUCTION

This appendix describes the VERSAbus pin connections. The following table identifies the VERSAbus signals by signal mnemonic, connector and pin number, and signal characteristic. Unless otherwise specified, all signal lines are driven by the master.

VERSAbus Signal Identification

SIGNAL MNEMONIC	CONNECTOR AND PIN NUMBER	SIGNAL NAME AND DESCRIPTION
ACCLK	J1: 69	AC CLOCK - Open collector driven clock signal generated by the power monitor that indicates the power line frequency and zero voltage transition points.
ACFAIL*	J1: 78	AC FAILURE - Open-collector driven signal which indicates that the AC input to the power supply is no longer being provided or that the required input voltage levels are not being met.
ACKIN*	J1: 95	ACKNOWLEDGE IN - Totem-pole driven signal. ACKIN* and ACKOUT* signals form a daisy-chained acknowledge. The ACKIN* signal indicates to VERSAboard that an acknowledge cycle is in progress.
ACKOUT*	J1: 96	ACKNOWLEDGE OUT - Totem-pole driven signal. ACKIN* and ACKOUT* signals form a daisy-chained acknowledge. The ACKOUT* signal indicates to the next board that an acknowledge cycle is in progress.
AM0*-AM7*	J1: 59,60, 63,83-86, 94	ADDRESS MODIFIER (bits 0-7) - Three-state driven lines that provide additional information about the address bus - such as size, cycle type, and/or DTB master identification.
APARITY0*	J1: 33	ADDRESS PARITY 0 - Three-state driven signal which provides an even parity bit for address bits A01*-A23*, LWORD*, and AM0*-AM7*.
APARITY1*	J2: 88	ADDRESS PARITY 1 - Three-state driven signal which provides an even parity bit for address bits A24*-A31* for use in 32-bit expansion.

VERSAbus Signal Identification (cont'd)

SIGNAL MNEMONIC	CONNECTOR AND PIN NUMBER	SIGNAL NAME AND DESCRIPTION
APVAL*	J1: 117	ADDRESS PARITY VALID - Three-state driven signal that indicates that valid parity has been placed on the appropriate APARITY lines.
AS*	J1: 30	ADDRESS STROBE - Three-state driven signal that indicates a valid address is on the address bus.
A01*-A23*	J1: 36-58	ADDRESS bus (bits 1-23) - Three-state driven address lines that specify a memory address.
A24*-A31*	J2: 89-96	ADDRESS bus (bits 24-31) - Three-state driven optional address lines that specify an extended memory address.
BBSY*	J1: 112	BUS BUSY - Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BCLR*	J1: 113	BUS CLEAR - Totem-pole driven signal generated by the bus arbitrator to request release by the current DTB master in the event that a higher level is requesting the bus.
BERR*	J1: 81	BUS ERROR - Open-collector driven signal generated by a slave. This signal indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BG0IN*-BG4IN*	J1: 97,99, 101,103, 105	BUS GRANT (0-4) IN - Totem-pole driven signals generated by the Arbiter or Requesters. Bus grant in and out signals form a daisy-chained bus grant. The bus grant signal indicates to this board that it may become the next bus master.
BG0OUT*-BG4OUT*	J1: 98,100, 102,104, 106	BUS GRANT (0-4) OUT - Totem-pole driven signals generated by Requesters. Bus grant in and out signals form a daisy-chained bus grant. The bus grant out signal indicates to the next board that it may become the next bus master.
BR0*-BR4*	J1: 107-111	BUS REQUEST (0-4) - Open-collector driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.
BREL*	J1: 114	BUS RELEASE - Open-collector driven signal generated by an emergency requester to indicate to the current DTB master that the master must clear the bus within 16 data transfer cycles. It also informs the arbiter that a highest priority bus request exists.

VERSAbus Signal Identification (cont'd)

SIGNAL MNEMONIC	CONNECTOR AND PIN NUMBER	SIGNAL NAME AND DESCRIPTION
DPARITY0*	J1: 21	DATA PARITY 0 - Three-state driven bidirectional signal, generated by either the master or the slave, which provides an even parity bit for data bits D00*-D07*.
DPARITY1*	J1: 22	DATA PARITY 1 - Three-state driven bidirectional signal, generated by either the master or the slave, which provides an even parity bit for data bits D08*-D15*.
DPARITY2*	J2: 103	DATA PARITY 2 - Three-state driven bidirectional signal, generated by either the master or the slave, which provides an even parity bit for data bus D16*-D23*.
DPARITY3*	J2: 104	DATA PARITY 3 -Three-state driven bidirectional signal, generated by either the master or the slave, which which provides an even parity bit for data bits D24*-D31*.
DPVAL*	J1: 118	DATA PARITY VALID - Three-state driven bidirectional signal that indicates during a data transfer that valid parity has been placed on the appropriate DPARITY lines.
DS0*	J1: 25	DATA STROBE 0 - Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D00*-D07*).
DS1*	J1: 26	DATA STROBE 1 - Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D08*-D15*).
DTACK*	J1: 29	DATA TRANSFER ACKNOWLEDGE - Open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
D00*-D15*	J1: 5-20	DATA BUS (bits 0-15) - Three-state driven bidirectional data lines that provide a data path between the DTB master and slave.
D16*-D31*	J2: 105-120	DATA BUS (bits 16-31) - Three-state driven bidirectional data lines that provide an expanded data path between the DTB master and slave for the optional expanded data bus configuration (option EADB).

VERSAbus Signal Identification (cont'd)

SIGNAL MNEMONIC	CONNECTOR AND PIN NUMBER	SIGNAL NAME AND DESCRIPTION
GND	J1: 3,4,23, 24,27,28, 31,32,61, 62,67,68, 71,72, 119,120, 123,124, 135-140	GROUND
GND	J2: 1-6	GROUND
GND	J2: 97,98, 101,102	GROUND (EXPANDED BUS OPTION ONLY)
GND (±15V)	J2: 13,14	ANALOG GROUND
[I/O PIN]	J2: 17-66	INPUT/OUTPUT PIN - I/O signal lines set aside for user peripheral interfacing applications on expanded bus backplanes.
	J2: 17-66, 71-120	INPUT/OUTPUT PIN - I/O signal lines set aside for user peripheral interfacing applications on non-expanded bus backplanes.
IRQ1*-IRQ7*	J1: 87-93	INTERRUPT REQUEST (1-7) - Open-collector driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven is the highest priority.
LWORD*	J1: 35	LONGWORD - Three-state driven signal specifying that the cycle is a byte/word transfer (when high) or a longword transfer (when low). LONGWORD transfers are only possible between an option D32 MASTER and an option D32 SLAVE using an expanded backplane.
[RESERVED]	J1: 64,66, 73,75,76, 77,82, 115-116	RESERVED - Signal lines reserved for future VERSAbus enhancements These lines must not be used by users.
	J2: 71-87, 99,100	RESERVED - (EXPANDED BUS backplanes ONLY.)
SYSCLK	J1: 70	SYSTEM CLOCK - A constant 16 MHz clock signal that is independent of processor speed or timing. This signal is used for general system timing use.

VERSAbus Signal Identification (cont'd)

SIGNAL MNEMONIC	CONNECTOR AND PIN NUMBER	SIGNAL NAME AND DESCRIPTION
SYSFAIL*	J1: 80	SYSTEM FAIL - Open-collector driven signal that indicates that a failure has occurred in the system. This signal may be generated by any module on the VERSAbus.
SYSRESET*	J1: 74	SYSTEM RESET - Open-collector driven signal which, when low, will cause the system to be reset.
TEST0*- TEST1*	J1: 65 79	SYSTEM TEST - Open collector driven signals that specify the mode to be entered when the SYSRESET* line is released.
WRITE*	J1: 34	WRITE - Three-state driven signal that specifies the data transfer cycle in progress to be either read or write. A high level indicates a read operation; a low level indicates a write operation.
+5V STDBY	J1: 133-134	+5 Vdc STANDBY - This line supplies +5 Vdc to devices requiring battery backup.
+5V	J1: 1,2, 129-132 J2: 7-10	+5 Vdc Power - Used by system logic circuits.
+12V	J1: 125-128 J2: 11,12	+12 Vdc Power - Used by system logic circuits.
+15V	J2: 69,70	+15 Vdc Power - Used by system analog circuits.
-12V	J1: 121,122 J2: 15,16	-12 Vdc Power - Used by system logic circuits.
-15V	J2: 67,68	-15 Vdc Power - Used by system analog circuits.

APPENDIX D

VERSAbus BACKPLANE EDGE CONNECTOR J1
AND
VERSAboard EDGE CONNECTOR P1
IDENTIFICATION

INTRODUCTION

This appendix identifies the VERSAbus backplane edge connector J1/P1 pin assignments. The following table lists the pin assignments by pin number order.

J1/P1 Pin Assignments

ODD PIN NUMBER (P1 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P1 SOLDER SIDE)	SIGNAL MNEMONIC
1	+5V	2	+5V
3	GND	4	GND
5	D00*	6	D01*
7	D02*	8	D03*
9	D04*	10	D05*
11	D06*	12	D07*
13	D08*	14	D09*
15	D10*	16	D11*
17	D12*	18	D13*
19	D14*	20	D15*
21	DPARITY0*	22	DPARITY1*
23	GND	24	GND
25	DS0*	26	DS1*
27	GND	28	GND
29	DTACK*	30	AS*
31	GND	32	GND
33	APARITY0*	34	WRITE*
35	LWORD*	36	A01*
37	A02*	38	A03*
39	A04*	40	A05*
41	A06*	42	A07*
43	A08*	44	A09*
45	A10*	46	A11*
47	A12*	48	A13*
49	A14*	50	A15*
51	A16*	52	A17*
53	A18*	54	A19*
55	A20*	56	A21*
57	A22*	58	A23*
59	AM4*	60	AM7*
61	GND	62	GND
63	AM3*	64	[RESERVED]
65	TEST0*	66	[RESERVED]

J1/P1 Pin Assignments (cont'd)

ODD PIN NUMBER (P1 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P1 SOLDER SIDE)	SIGNAL MNEMONIC
67	GND	68	GND
69	ACCLK	70	SYSCLK
71	GND	72	GND
73	[RESERVED]	74	SYSRESET*
75	[RESERVED]	76	[RESERVED]
77	[RESERVED]	78	ACFAIL*
79	TEST1*	80	SYSFAIL*
81	BERR*	82	[RESERVED]
83	AM0*	84	AM1*
85	AM2*	86	AM6*
87	IRQ1*	88	IRQ2*
89	IRQ3*	90	IRQ4*
91	IRQ5*	92	IRQ6*
93	IRQ7*	94	AM5*
95	ACKIN*	96	ACKOUT*
97	BGOIN*	98	BGOOUT*
99	BG1IN*	100	BG1OUT*
101	BG2IN*	102	BG2OUT*
103	BG3IN*	104	BG3OUT*
105	BG4IN*	106	BG4OUT*
107	BRO*	108	BR1*
109	BR2*	110	BR3*
111	BR4*	112	BBSY*
113	BCLR*	114	BREL*
115	[RESERVED]	116	[RESERVED]
117	APVAL*	118	DPVAL*
119	GND	120	GND
121	-12V	122	-12V
123	GND	124	GND
125	+12V	126	+12V
127	+12V	128	+12V
129	+5V	130	+5V
131	+5V	132	+5V
133	+5V STDBY	134	+5V STDBY
135	GND	136	GND
137	GND	138	GND
139	GND	140	GND

APPENDIX E

VERSAbus BACKPLANE EDGE CONNECTOR J2

AND

VERSAboard EDGE CONNECTOR P2

IDENTIFICATION

INTRODUCTION

This appendix identifies the VERSAbus backplane edge connector J2 pin assignments. Table 1 lists the J2/P2 pin assignments by pin number order for the expanded bus option. Table 2 lists the J2/P2 pin assignments for the non-expanded bus option.

TABLE 1. J2/P2 Pin Assignments for the Expanded Bus Option

ODD PIN NUMBER (P2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P2 SOLDER SIDE)	SIGNAL MNEMONIC
1	GND	2	GND
3	GND	4	GND
5	GND	6	GND
7	+5V	8	+5V
9	+5V	10	+5V
11	+12V	12	+12V
13	GND (± 15V)	14	GND (± 15V)
15	-12V	16	-12V
17	[I/O PIN]	18	[I/O PIN]
19	[I/O PIN]	20	[I/O PIN]
21	[I/O PIN]	22	[I/O PIN]
23	[I/O PIN]	24	[I/O PIN]
25	[I/O PIN]	26	[I/O PIN]
27	[I/O PIN]	28	[I/O PIN]
29	[I/O PIN]	30	[I/O PIN]
31	[I/O PIN]	32	[I/O PIN]
33	[I/O PIN]	34	[I/O PIN]
35	[I/O PIN]	36	[I/O PIN]
37	[I/O PIN]	38	[I/O PIN]
39	[I/O PIN]	40	[I/O PIN]
41	[I/O PIN]	42	[I/O PIN]
43	[I/O PIN]	44	[I/O PIN]
45	[I/O PIN]	46	[I/O PIN]
47	[I/O PIN]	48	[I/O PIN]
49	[I/O PIN]	50	[I/O PIN]
51	[I/O PIN]	52	[I/O PIN]
53	[I/O PIN]	54	[I/O PIN]
55	[I/O PIN]	56	[I/O PIN]
57	[I/O PIN]	58	[I/O PIN]
59	[I/O PIN]	60	[I/O PIN]

TABLE 1. J2/P2 Pin Assignments for the Expanded Bus Option (cont'd)

ODD PIN NUMBER (P2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P2 SOLDER SIDE)	SIGNAL MNEMONIC
61	[I/O PIN]	62	[I/O PIN]
63	[I/O PIN]	64	[I/O PIN]
65	[I/O PIN]	66	[I/O PIN]
67	-15V	68	-15V
69	+15V	70	+15V
71	[RESERVED]	72	[RESERVED]
73	[RESERVED]	74	[RESERVED]
75	[RESERVED]	76	[RESERVED]
77	[RESERVED]	78	[RESERVED]
79	[RESERVED]	80	[RESERVED]
81	[RESERVED]	82	[RESERVED]
83	[RESERVED]	84	[RESERVED]
85	[RESERVED]	86	[RESERVED]
87	[RESERVED]	88	APARITY1*
89	A24*	90	A25*
91	A26*	92	A27*
93	A28*	94	A29*
95	A30*	96	A31*
97	GND	98	GND
99	[RESERVED]	100	[RESERVED]
101	GND	102	GND
103	DPARITY2*	104	DPARITY3*
105	D16*	106	D17*
107	D18*	108	D19*
109	D20*	110	D21*
111	D22*	112	D23*
113	D24*	114	D25*
115	D26*	116	D27*
117	D28*	118	D29*
119	D30*	120	D31*

NOTE: Pins 17 through 66 are not bussed together by the backplane.

TABLE 2. J2/P2 Pin Assignments for the Non-Expanded Bus Option

ODD PIN NUMBER (P2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P2 SOLDER SIDE)	SIGNAL MNEMONIC
1	GND	2	GND
3	GND	4	GND
5	GND	6	GND
7	+5V	8	+5V
9	+5V	10	+5V
11	+12V	12	+12V
13	GND (± 15V)	14	GND (± 15V)
15	-12V	16	-12V
17	[I/O PIN]	18	[I/O PIN]
19	[I/O PIN]	20	[I/O PIN]
21	[I/O PIN]	22	[I/O PIN]
23	[I/O PIN]	24	[I/O PIN]
25	[I/O PIN]	26	[I/O PIN]
27	[I/O PIN]	28	[I/O PIN]
29	[I/O PIN]	30	[I/O PIN]
31	[I/O PIN]	32	[I/O PIN]
33	[I/O PIN]	34	[I/O PIN]
35	[I/O PIN]	36	[I/O PIN]
37	[I/O PIN]	38	[I/O PIN]
39	[I/O PIN]	40	[I/O PIN]
41	[I/O PIN]	42	[I/O PIN]
43	[I/O PIN]	44	[I/O PIN]
45	[I/O PIN]	46	[I/O PIN]
47	[I/O PIN]	48	[I/O PIN]
49	[I/O PIN]	50	[I/O PIN]
51	[I/O PIN]	52	[I/O PIN]
53	[I/O PIN]	54	[I/O PIN]
55	[I/O PIN]	56	[I/O PIN]
57	[I/O PIN]	58	[I/O PIN]
59	[I/O PIN]	60	[I/O PIN]
61	[I/O PIN]	62	[I/O PIN]
63	[I/O PIN]	64	[I/O PIN]
65	[I/O PIN]	66	[I/O PIN]
67	-15V	68	-15V
69	+15V	70	+15V
71	[I/O PIN]	72	[I/O PIN]
73	[I/O PIN]	74	[I/O PIN]
75	[I/O PIN]	76	[I/O PIN]
77	[I/O PIN]	78	[I/O PIN]
79	[I/O PIN]	80	[I/O PIN]
81	[I/O PIN]	82	[I/O PIN]
83	[I/O PIN]	84	[I/O PIN]
85	[I/O PIN]	86	[I/O PIN]
87	[I/O PIN]	88	[I/O PIN]
89	[I/O PIN]	90	[I/O PIN]
91	[I/O PIN]	92	[I/O PIN]
93	[I/O PIN]	94	[I/O PIN]
95	[I/O PIN]	96	[I/O PIN]

TABLE 2. J2/P2 Pin Assignments for the Non-Expanded Bus Option (cont'd)

ODD PIN NUMBER (P2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P2 SOLDER SIDE)	SIGNAL MNEMONIC
97	[I/O PIN]	98	[I/O PIN]
99	[I/O PIN]	100	[I/O PIN]
101	[I/O PIN]	102	[I/O PIN]
103	[I/O PIN]	104	[I/O PIN]
105	[I/O PIN]	106	[I/O PIN]
107	[I/O PIN]	108	[I/O PIN]
109	[I/O PIN]	110	[I/O PIN]
111	[I/O PIN]	112	[I/O PIN]
113	[I/O PIN]	114	[I/O PIN]
115	[I/O PIN]	116	[I/O PIN]
117	[I/O PIN]	118	[I/O PIN]
119	[I/O PIN]	120	[I/O PIN]

NOTE: Pins 17 through 66 and pins 71 through 120 are not bussed together by the backplane.

BUS DRIVER AND RECEIVER SUMMARY

SIGNAL MNEMONIC	SIGNAL NAME	DRIVER TYPE	DRIVER MODULE	RECEIVER MODULE	TERMINATION NETWORK
A01*-A31* (31 lines)	ADDRESS BUS	THREE	MASTERS, INTERRUPT HANDLERS	SLAVES, INTERRUPTERS	YES
AM0*-AM7* (8 lines)	ADDRESS MODIFIER				
AS*	ADDRESS STROBE				
LWORD*	LONGWORD				
WRITE*	WRITE				
DS0*-DS1* (2 lines)	DATA STROBES				
D00*-D31* (32 lines)	DATA BUS	THREE	MASTERS, SLAVES, INTERRUPTERS	SLAVES, MASTERS, INTERRUPT HANDLERS	YES
DTACK*	DATA TRANSFER ACKNOWEDGE	OC	SLAVES, INTERRUPTERS	MASTERS, INTERRUPT HANDLERS	YES
BERR*	BUS ERROR	OC	SLAVES	MASTERS	YES
DPARITY0*-DPARITY3* (4 lines)	DATA PARITY	THREE	DP MASTERS DP SLAVES	DP SLAVES DP MASTERS	YES
DPVAL*	DATA PARITY VALID	THREE	DP MASTERS DP SLAVES	DP MASTERS DP SLAVES	YES
APARITY0*-APARITY1* (2 lines)	ADDRESS PARITY	THREE	AP MASTERS	AP SLAVES	YES
APVAL*	ADDRESS PARITY VALID	THREE	AP MASTERS	AP SLAVES	YES

APPENDIX F

DC SIGNAL SPECIFICATION

This appendix provides a summary showing which signal lines on VERSAbus are driven/received by each functional module, and the type of driver each uses.

In order to simplify the table, an abbreviated notation is used to describe the various types of drivers. The notations used are shown below:

Totem pole (high current)	- TP HC
Totem pole (low current)	- TP LC
Three-state	- THREE
Open collector	- OC

For the driver specifications, see Table 7-2 in Chapter 7.

All functional modules use the same type of receiver. (For the receiver specifications, see Table 7-3 in Chapter 7.)

BUS DRIVER AND RECEIVER SUMMARY (cont'd)

SIGNAL MNEMONIC	SIGNAL NAME	DRIVER TYPE	DRIVER MODULE	RECEIVER MODULE	TERMINATION NETWORK
BR0*-BR4* (5 lines)	BUS REQUEST	OC	REQUESTERS	ARBITER	YES
BG0IN*-BG4IN* (5 lines)	BUS GRANT	TP LC	ARBITER	REQUESTERS	NO
BG0OUT*-BG4OUT* (5 lines)			REQUESTERS	(NOT APPLICABLE)	NO
BBSY*	BUS BUSY	OC	EMERGENCY REQUESTER	ARBITER	YES
BCLR*	BUS CLEAR	TP HC	ARBITER	MASTERS	YES
BREL*	BUS RELEASE	TP HC	EMERGENCY REQUESTER	MASTERS	YES
IRQ1*-IRQ7* (7 lines)	INTERRUPT REQUEST	OC	INTERRUPTERS	INTERRUPT HANDLERS	YES
ACKIN*/ACKOUT*	ACKNOWLEDGE DAISY CHAIN	TP LC	INTERRUPT HANDLERS, INTERRUPTERS	INTERRUPTERS INTERRUPTERS	NO
SYSRESET*	SYSTEM RESET	OC	POWER MONITOR, MANUAL SWITCH	ANY ANY	YES
ACFAIL*	AC FAILURE	OC	POWER MONITOR	EMERGENCY REQUESTER	YES
ACCLK	AC CLOCK	OC	POWER MONITOR	ANY	YES
SYSCLK	SYSTEM CLOCK	TP HC	CLOCK DRIVER	ANY	YES
SYSFAIL*	SYSTEM FAIL	OC	MASTERS, SLAVES	ANY ANY	YES
TEST0*-TEST1* (2 lines)	SYSTEM TEST	OC	POWER MONITOR MANUAL SWITCH	ANY ANY	YES

11/26/85
ES11257-1 UNIDEX 16 SYSTEM CONFIGURATION
UNIDEX 16 CARD CAGE MOTHER BOARD
690D1218 (REV B)
CO#_____

A. COMMON/FRAME GROUND JUMPERS

STANDARD CONFIGURATION:

R1 = 100 Ohms, 1/2W Resistor
R2 = 0 Ohm Jumper

R1 and R2 connect Unidex 16 DC Power Supply Common to the Card Cage Frame. To isolate the Power Supply Common from the card cage frame, remove R1 and R2 as required.

B. FAULT SWITCH

The fault circuit is a series circuit that is daisy chained from module to module (A1 - A8). The circuit is fail safe, in that a fault will be reported if the circuit is open or if a module is not plugged into the mother board card slot. A fault is reported to Unidex 16 and the shut line will be asserted. Therefore, whenever a position (A1 - A8) is not used, the appropriate bypass switch must be closed to transfer the fault signal to the next module. The following lists the modules and corresponding switches:

ASSEMBLY#	SLOT	MODULE	SWITCH	ACTIVE	BYPASS
A1	S0	PWR.SUPPLY 690E1254	NO SWITCH	N/A	N/A
A2	S1	CPU BD. 690D1255	NO SWITCH	N/A	N/A
A3	S2	CRT BD. 690D1256	SW7-1	OFF	ON
A4*	S3	FDC BD. 690D1258	SW7-2	OFF	ON
A5*	S4	MEM BD. 690D1257	SW8-1	OFF	ON
A6*	S5	MEM BD. 690D1257	SW8-2	OFF	ON
A7*	S6	IDX BD. 690D1261	SW9-2	OFF	ON
A8	S7	IDX BD. 690D1261	NO SWITCH	N/A	N/A

EXAMPLE:

If the optional Indexing Board A7 is not used, switch SW9-2 must be in the "ON" position and if it is used, it must be in the "OFF" position.

* Indicates an optional module

C. ACKNOWLEDGE SWITCH

The acknowledge signal is an interlocking type signal that is daisy chained from one module (A1-A8) to the next. If a module is absent, the appropriate bypass switch (SW1-SW5) must be closed to transfer the signal to the next module. Failure to do so will cause a bus error. The following is a list of Unidex 16 assemblies, their normal positions on the bus, and their appropriate bypass switch.

ASSEMBLY#	SLOT	MODULE	SWITCH	ACTIVE	BYPASS
A1	S0	PWR.SUPPLY 690E1254	NO SWITCH	N/A	N/A
A2	S1	CPU BD. 690D1255	NO SWITCH	N/A	N/A
A3	S2	CRT BD. 690D1256	SW1-1	OFF	ON
A4*	S3	FDC BD. 690D1258	SW2-1	OFF	ON
A5*	S4	MEM BD. 690D1257	SW3-1	OFF	ON
A6*	S5	MEM BD. 690D1257	SW4-1	OFF	ON
A7*	S6	IDX BD. 690D1261	SW5-1	OFF	ON
A8	S7	IDX BD. 690D1261	NO SWITCH	N/A	N/A

EXAMPLE:

When Unidex 16 is used without the floppy disk control option (FDC A4), the bypass switch (SW2-1) must be in the "ON" position and if used with the FDC option, the bypass switch (SW2-1) must be in the "OFF" position.

* Indicates optional module.

D. REMAINING SWITCHES

The remaining switches are reserved for future use and although they have no effect on Unidex 16 at this time, they should be in the "OFF" position unless otherwise specified.

E. FAULT INPUT J9-8

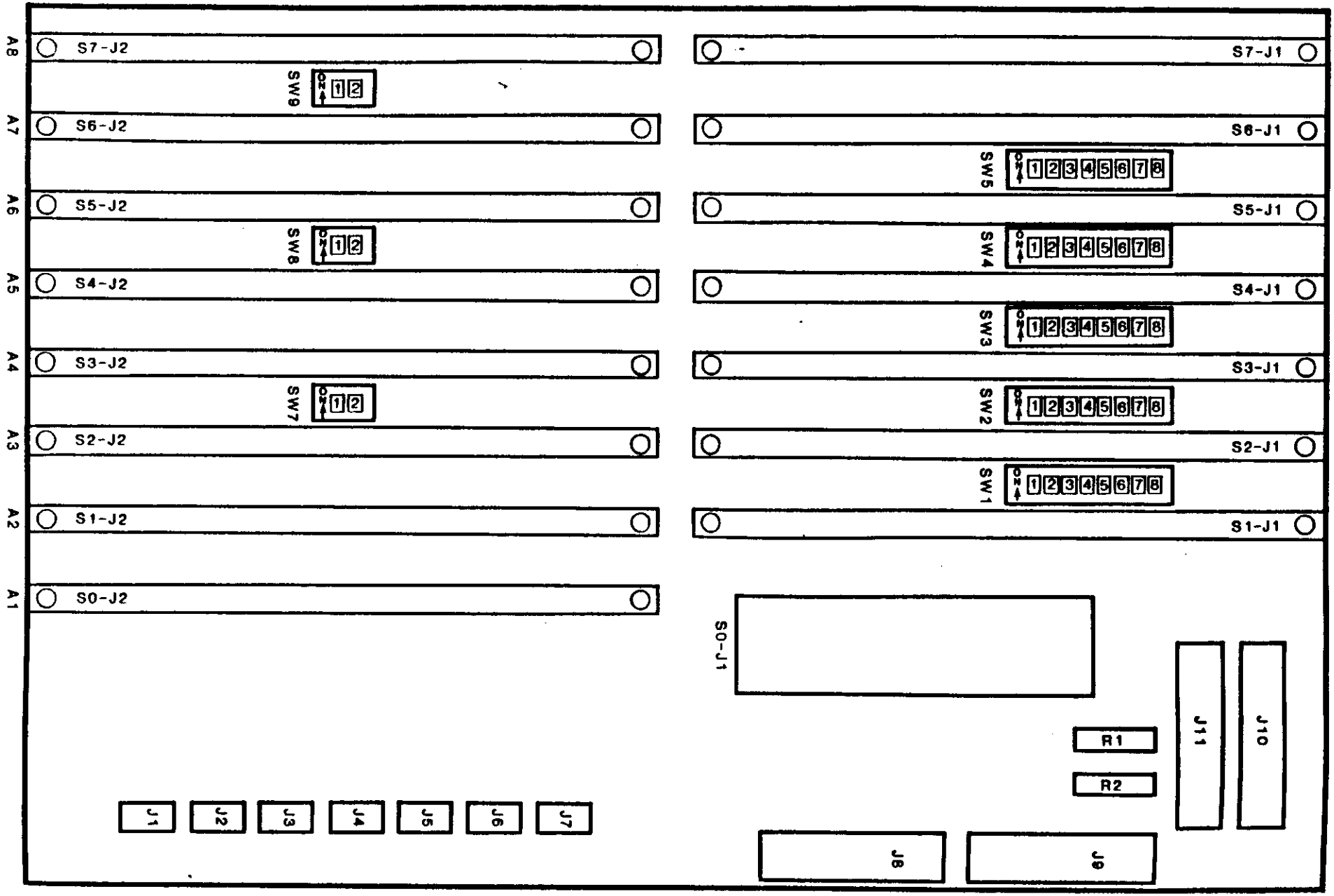
The fault input must be pulled low or a fault condition will exist that will inhibit normal system operation. If this input is not used, it can be jumpered to J9-1 (common).

F. FAULT OUTPUT J9-7

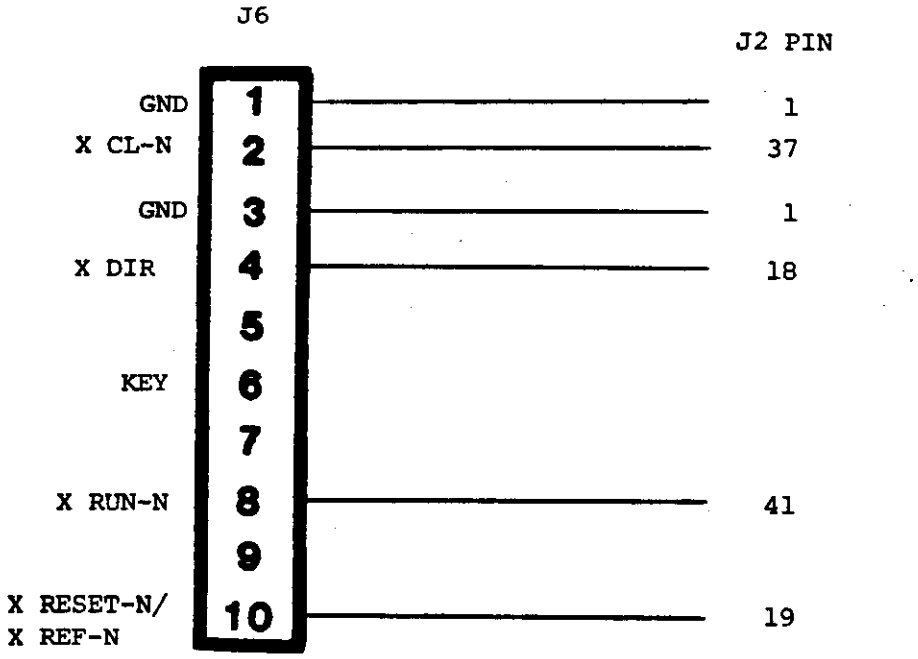
The fault output is normally low (open collector output) and is pulled high when a fault occurs. This output is usually tied to the shutdown input J9-6.

G. SHUTDOWN INPUT J9-6

The shutdown input J9-6 must be pulled low or a shutdown will occur. This input is normally tied to the fault output J9-7.

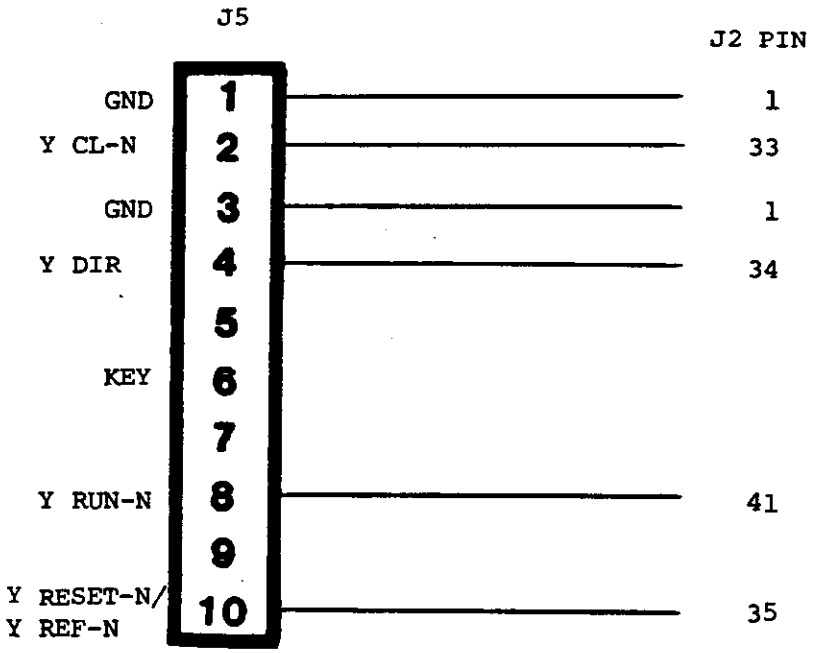

A8
S7-J2
SW9
ON 1 2
S7-J1
A7
S6-J2
S6-J1
SW5
ON 1 2 3 4 5 6 7 8
A6
S5-J2
S5-J1
SW6
ON 1 2
SW4
ON 1 2 3 4 5 6 7 8
A5
S4-J2
S4-J1
SW3
ON 1 2 3 4 5 6 7 8
A4
S3-J2
S3-J1
SW7
ON 1 2
SW2
ON 1 2 3 4 5 6 7 8
A3
S2-J2
S2-J1
SW1
ON 1 2 3 4 5 6 7 8
A2
S1-J2
S1-J1
A1
S0-J2
S0-J1
R1
R2
J11
J10
J1
J2
J3
J4
J5
J6
J7
J8
J9

MOTHER BOARD



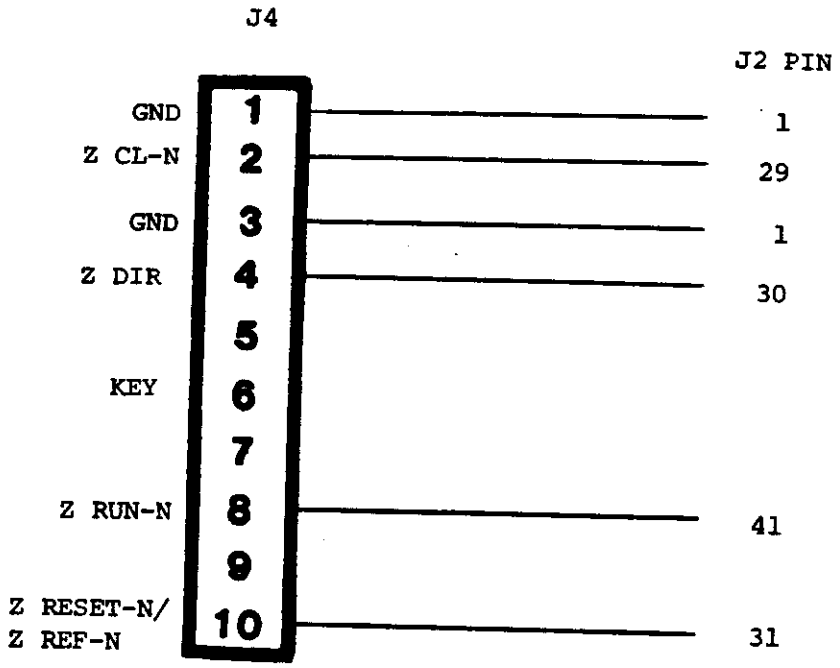
CONNECTOR

MOTHER BOARD



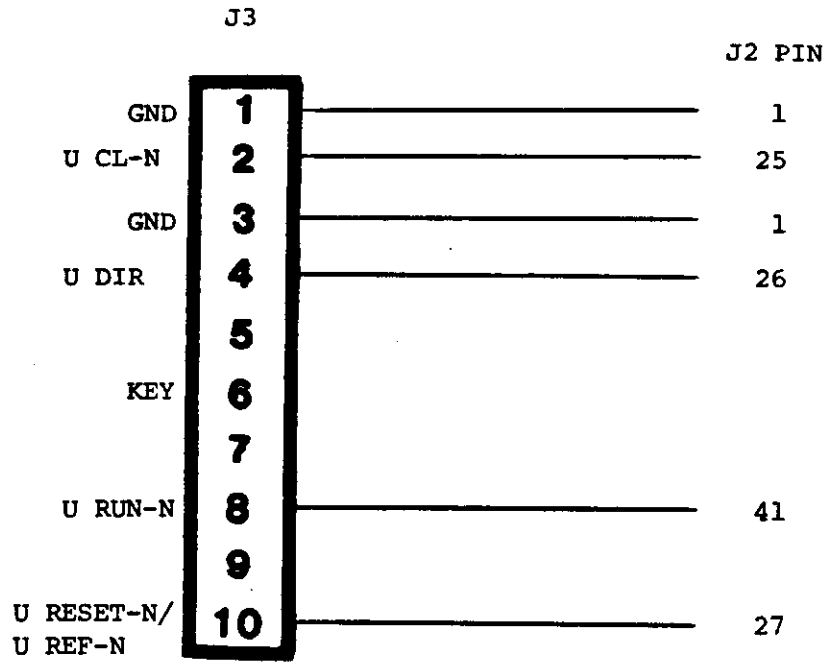
CONNECTOR

MOTHER BOARD



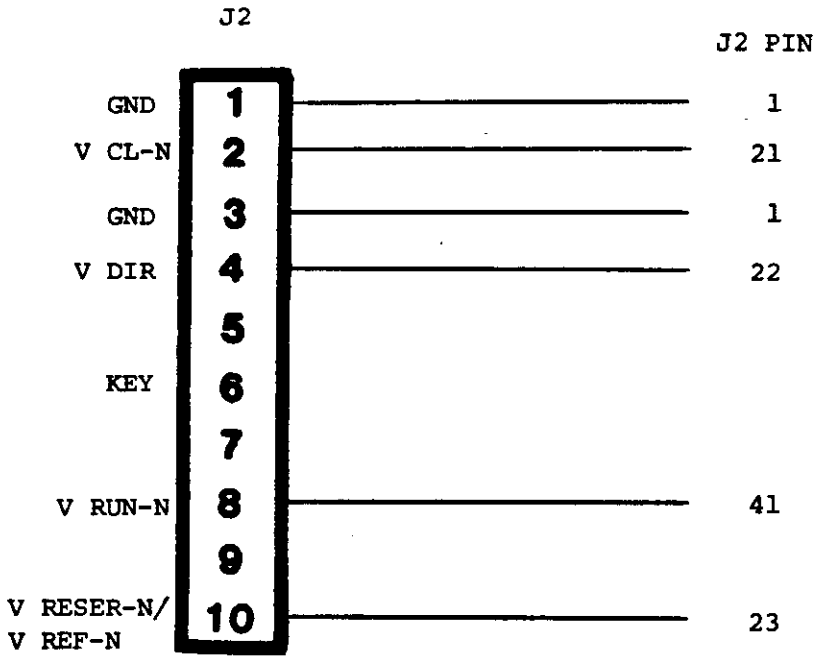
CONNECTOR

MOTHER BOARD



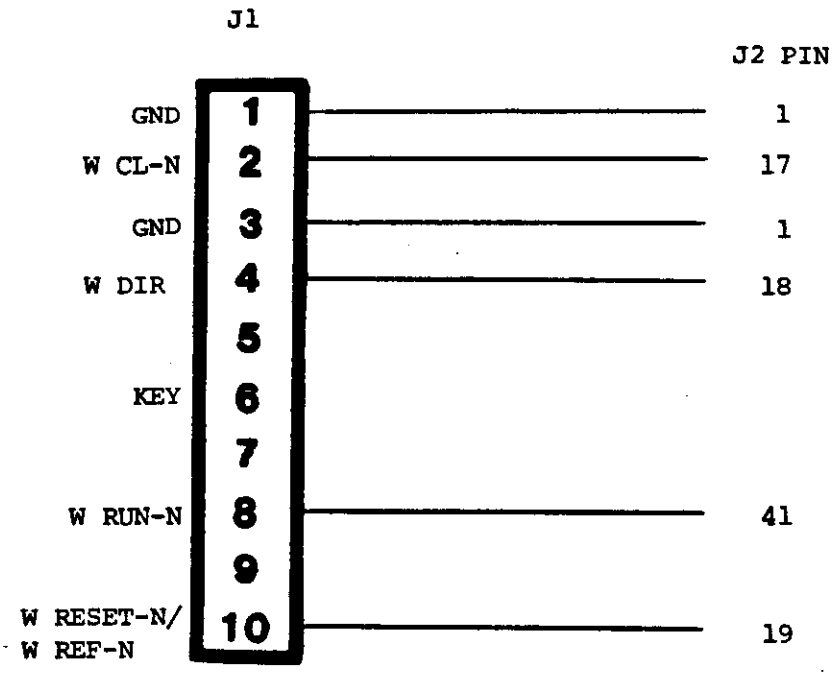
CONNECTOR

MOTHER BOARD



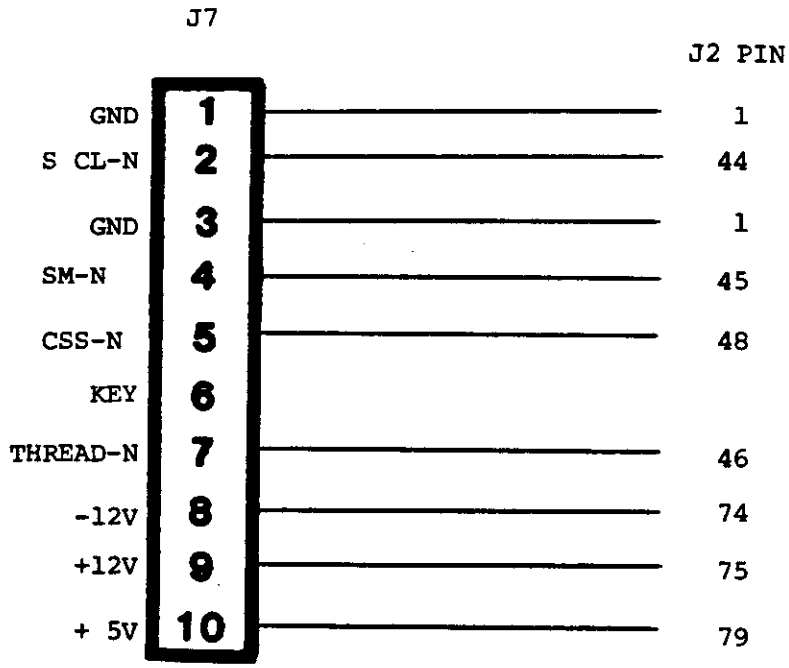
CONNECTOR

MOTHER BOARD



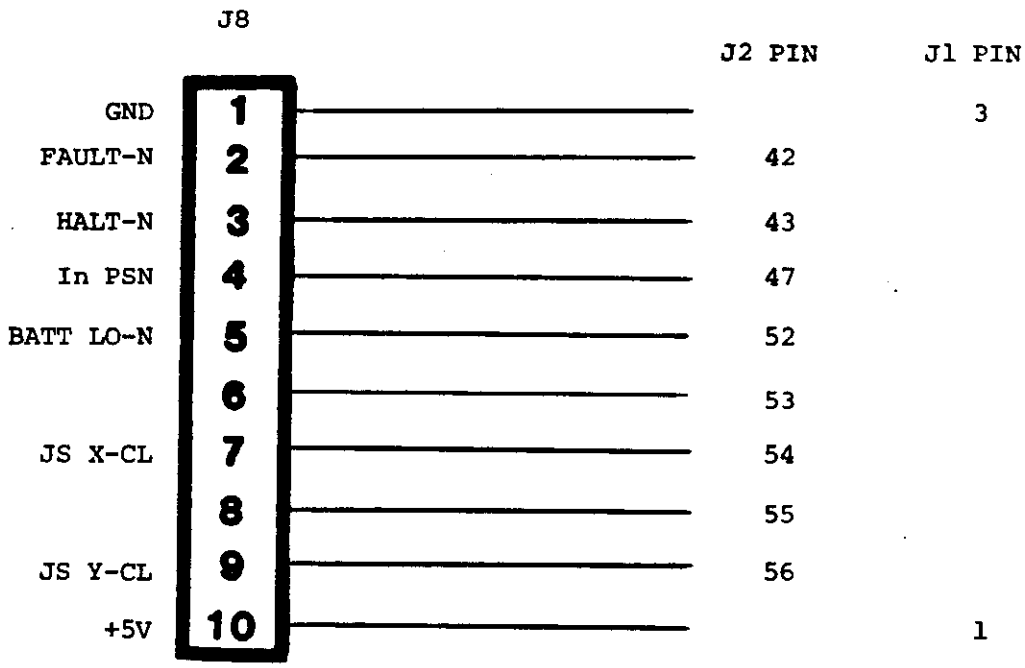
CONNECTOR

MOTHER BOARD



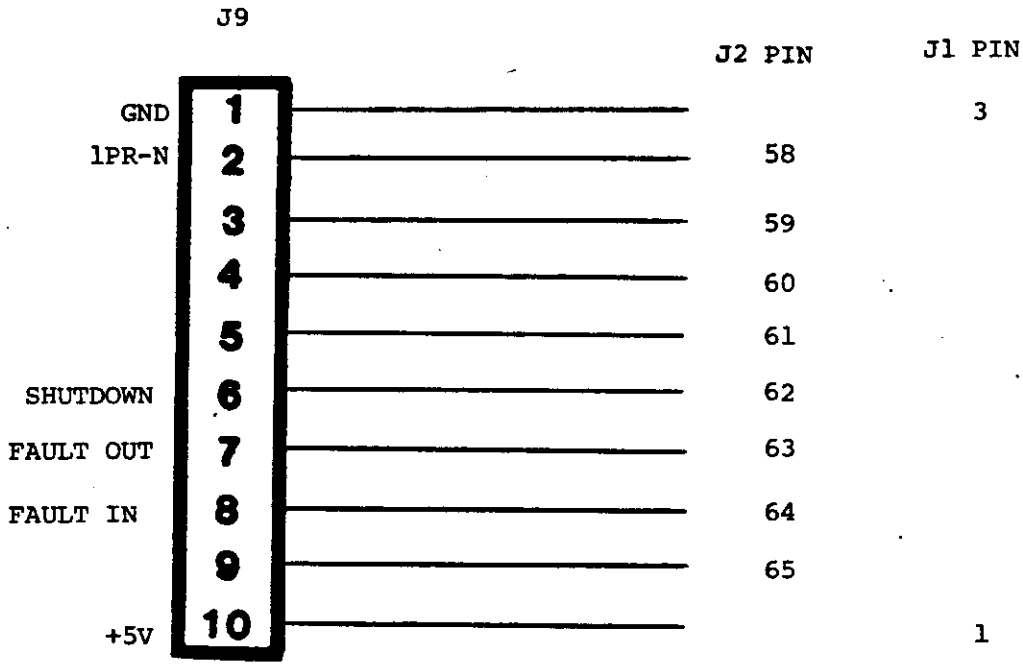
CONNECTOR

MOTHER BOARD



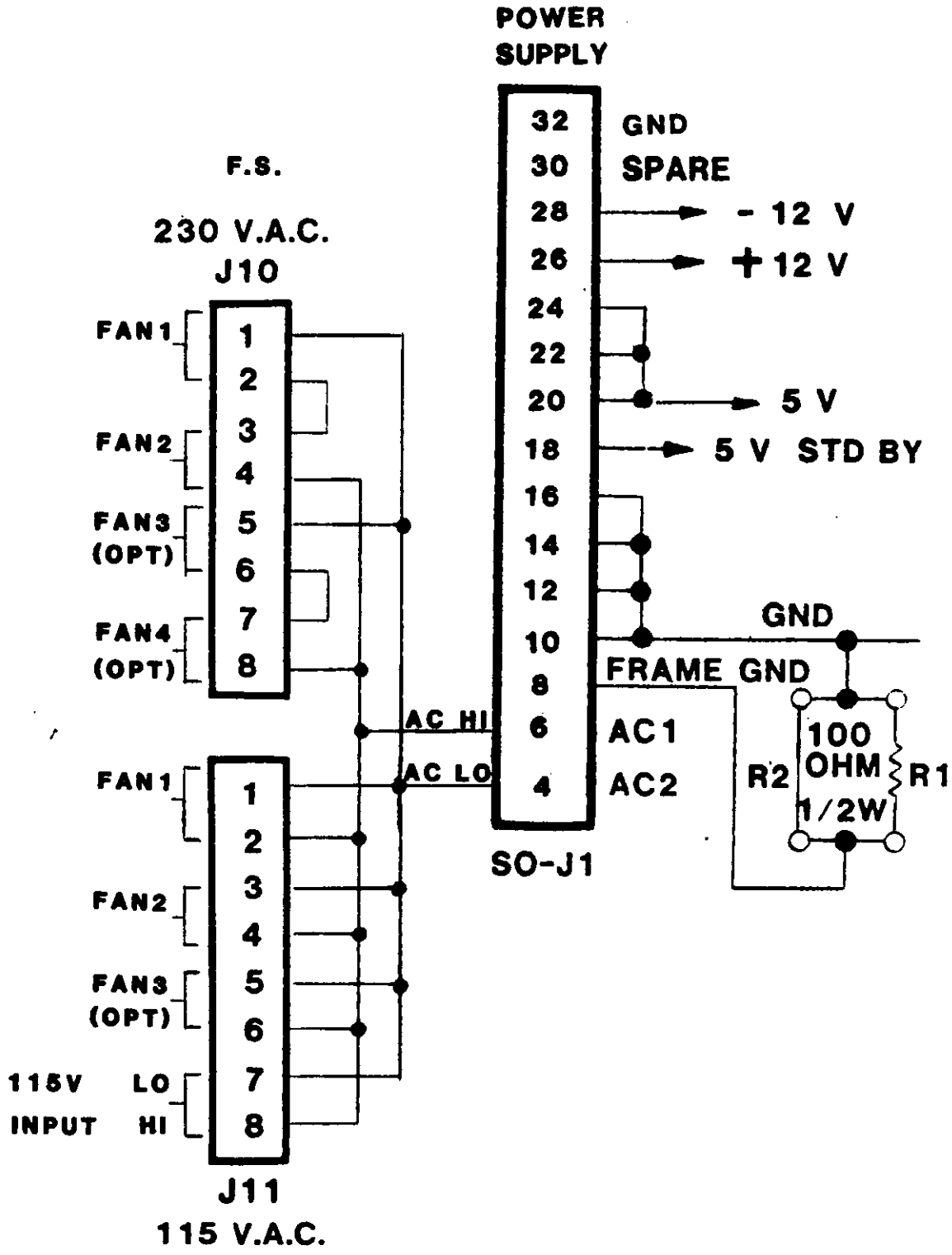
CONNECTOR

MOTHER BOARD



CONNECTOR

MOTHER BOARD



APPENDIX D

VERSAbus BACKPLANE EDGE CONNECTOR J1

AND

VERSAboard EDGE CONNECTOR P1

IDENTIFICATION

INTRODUCTION

This appendix identifies the VERSAbus backplane edge connector J1/P1 pin assignments. The following table lists the pin assignments by pin number order.

J1/P1 Pin Assignments

ODD PIN NUMBER (P1 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P1 SOLDER SIDE)	SIGNAL MNEMONIC
1	+5V	2	+5V
3	GND	4	GND
5	D00*	6	D01*
7	D02*	8	D03*
9	D04*	10	D05*
11	D06*	12	D07*
13	D08*	14	D09*
15	D10*	16	D11*
17	D12*	18	D13*
19	D14*	20	D15*
[illegible]	[illegible]	[illegible]	[illegible]
23	GND	24	GND
25	DS0*	26	DS1*
27	GND	28	GND
29	DTACK*	30	AS*
31	GND	32	GND
[illegible]	[illegible]	34	WRITE*
[illegible]	[illegible]	36	A01*
37	A02*	38	A03*
39	A04*	40	A05*
41	A06*	42	A07*
43	A08*	44	A09*
45	A10*	46	A11*
47	A12*	48	A13*
49	A14*	50	A15*
51	A16*	52	A17*
53	A18*	54	A19*
55	A20*	56	A21*
57	A22*	58	A23*
59	AM4*	[illegible]	[illegible]
61	GND	62	GND
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]

J1/P1 Pin Assignments (cont'd)

ODD PIN NUMBER (P1 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P1 SOLDER SIDE)	SIGNAL MNEMONIC
67	GND	68	GND
69	ACCLK	70	SYSCLK
71	GND	72	GND
[illegible]	[illegible]	74	SYSRESET*
[illegible]	[illegible]	76	[illegible]
[illegible]	[illegible]	78	ACFAIL*
[illegible]	[illegible]	[illegible]	[illegible]
81	BERR*	82	[RESERVED]
83	AM0*	84	AM1*
85	AM2*	86	AM6*
87	IRQ1*	88	IRQ2*
89	IRQ3*	90	IRQ4*
91	IRQ5*	92	IRQ6*
93	IRQ7*	94	AM5*
95	ACKIN*	96	ACKOUT*
97	BGOIN*	98	BGOOUT*
99	BG1IN*	100	BG1OUT*
101	BG2IN*	102	BG2OUT*
103	BG3IN*	104	BG3OUT*
105	BG4IN*	106	BG4OUT*
107	BR0*	108	BR1*
109	BR2*	110	BR3*
111	BR4*	112	BBSY*
113	BCLR*	114	BREL*
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
119	GND	120	GND
121	-12V	122	-12V
123	GND	124	GND
125	+12V	126	+12V
127	+12V	128	+12V
129	+5V	130	+5V
131	+5V	132	+5V
133	+5V STDBY	134	+5V STDBY
135	GND	136	GND
137	GND	138	GND
139	GND	140	GND

TABLE 2. J2/P2 Pin Assignments for the Non-Expanded Bus Option

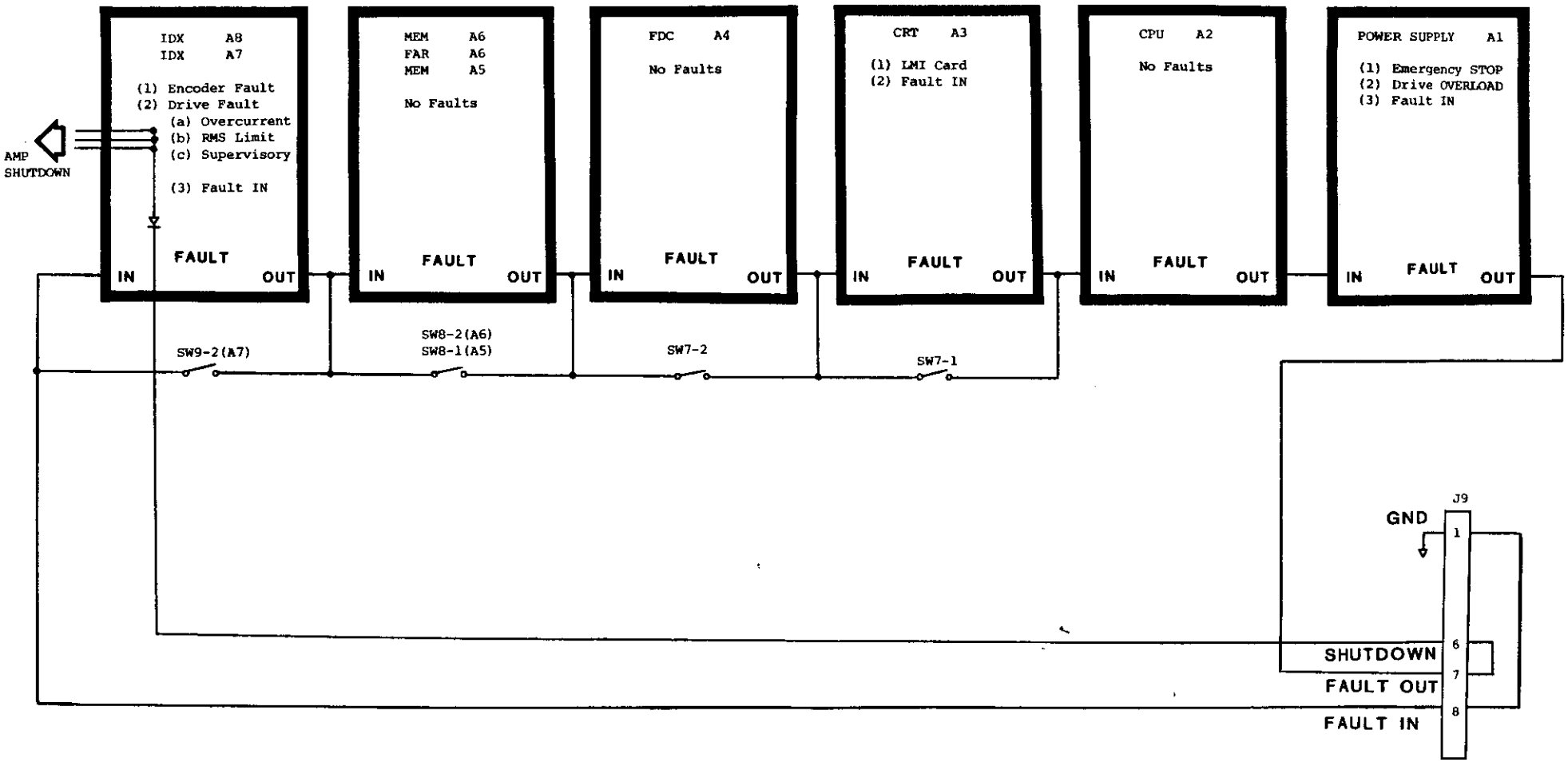
ODD PIN NUMBER (P2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P2 SOLDER SIDE)	SIGNAL MNEMONIC
1	GND	2	GND
3	GND	4	GND
5	GND	6	GND
7	+5V	8	+5V
9	+5V	10	+5V
11	+12V	12	+12V
13	GND (± 15V)	14	GND (± 15V)
15	-12V	16	-12V
17	W CL-N	18	W DIR
19	W RESET-N	20	{I/O PIN}
21	V CL-N	22	V DIR
23	V RESET-N	24	{I/O PIN}
25	U CL-N	26	U DIR
27	U RESET-N	28	{I/O PIN}
29	Z CL-N	30	Z DIR
31	Z RESET-N	32	{I/O PIN}
33	Y CL-N	34	Y DIR
35	Y RESET-N	36	{I/O PIN}
37	X CL-N	38	X DIR
39	X RESET-N	40	{I/O PIN}
41	RUN-N	42	FAULT-N
43	HALT-N	44	S CL-N
45	SM-N	46	THREAD-N
47	IN PSN	48	CSS-N
49	{I/O PIN}	50	{I/O PIN}
51	{I/O PIN}	52	BATT LO-N
53	{I/O PIN}	54	JS X CL
55	{I/O PIN}	56	JS Y CL
57	{I/O PIN}	58	1PR-N
59	{I/O PIN}	60	{I/O PIN}
61	{I/O PIN}	62	SHUTDOWN
63	FAULT OUT	64	FAULT IN
65	{I/O PIN}	66	FRAME GND
67	-15V	68	-15V
69	+15V	70	+15V
71	{I/O PIN}	72	{I/O PIN}

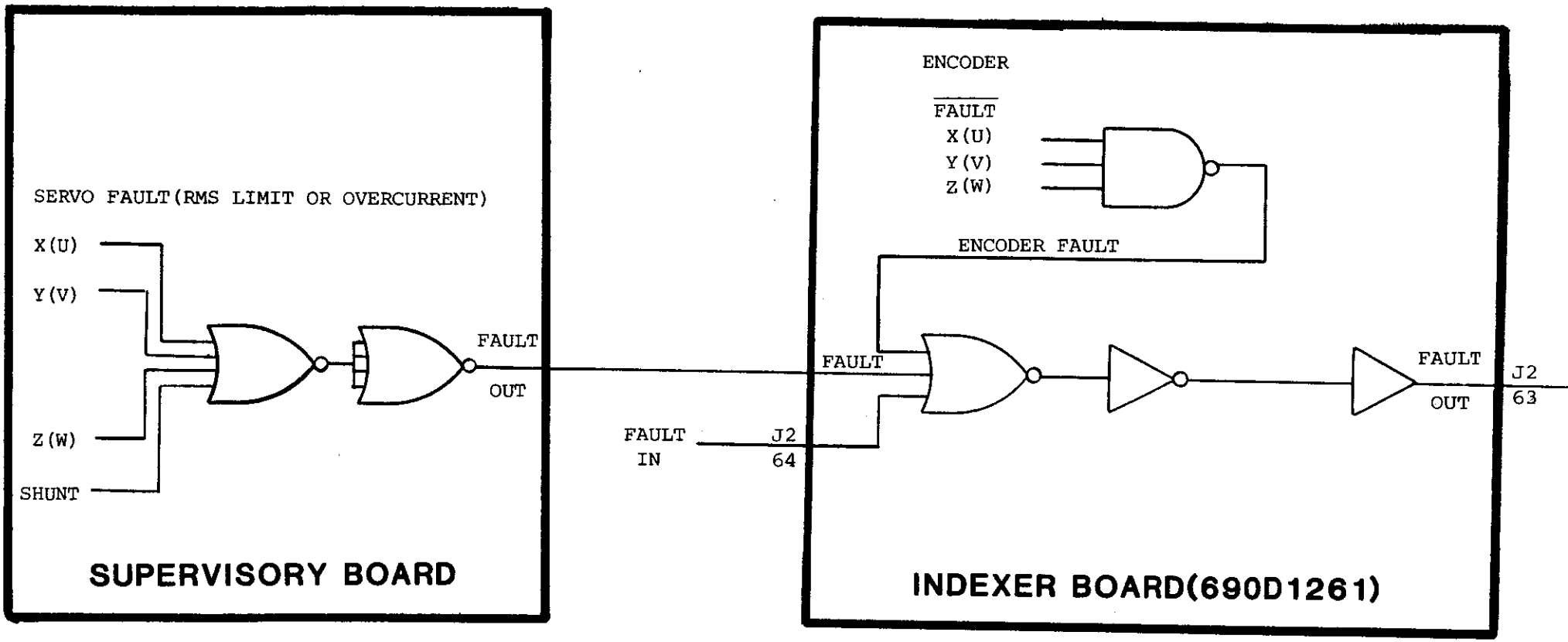
TABLE 2. J2/P2 Pin Assignments for the Non-Expanded Bus Option (cont'd)

ODD PIN NUMBER (P2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P2 SOLDER SIDE)	SIGNAL MNEMONIC
97	GND	98	GND
[illegible]	[illegible]	[illegible]	[illegible]
101	GND	102	GND
[illegible]	[illegible]	[illegible]	[illegible]

NOTE: Pins 17 through 66 and pins 71 through 120 are not bussed together by the backplane.

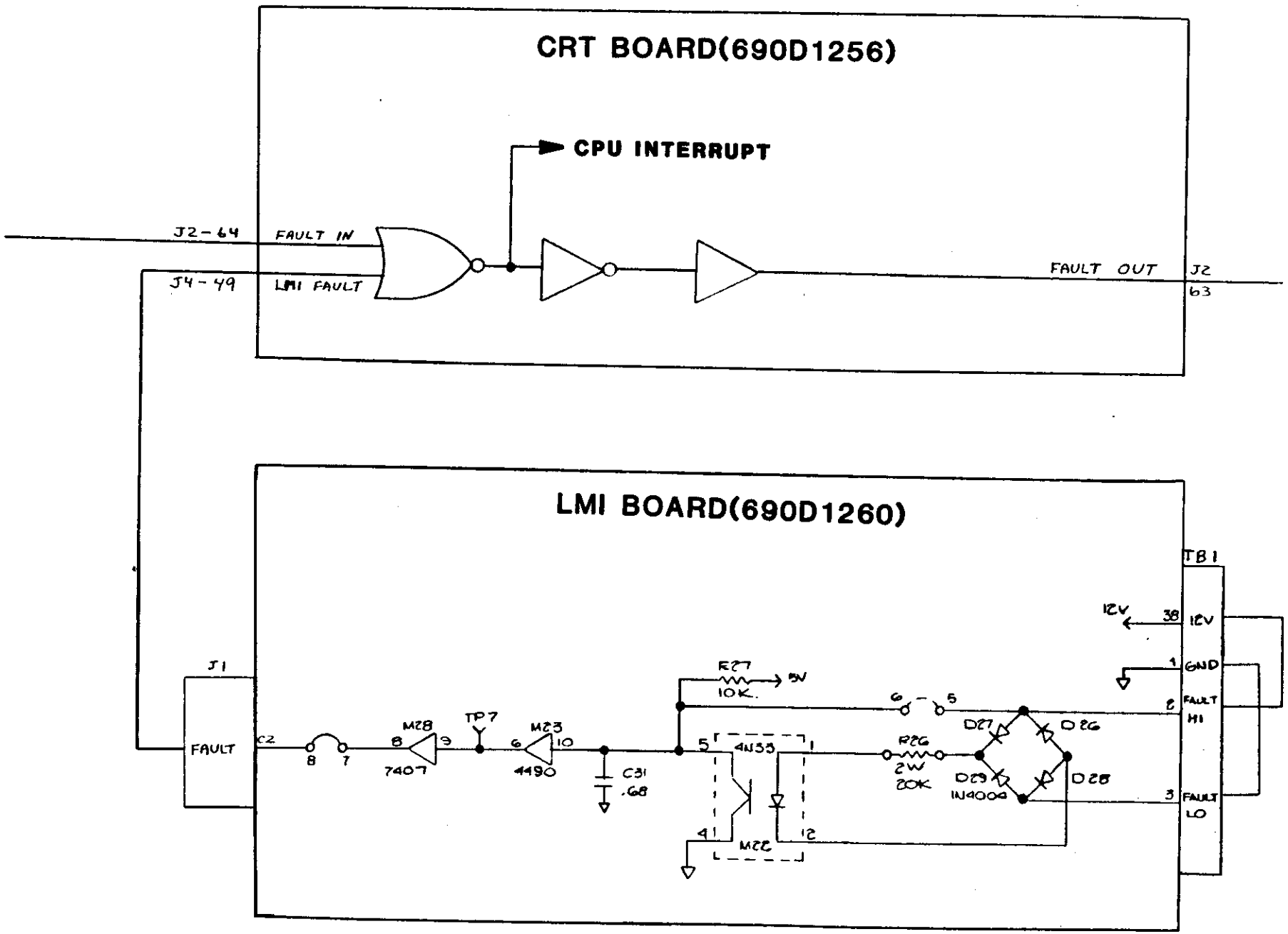
UNIDEX 16 FAULT CIRCUIT

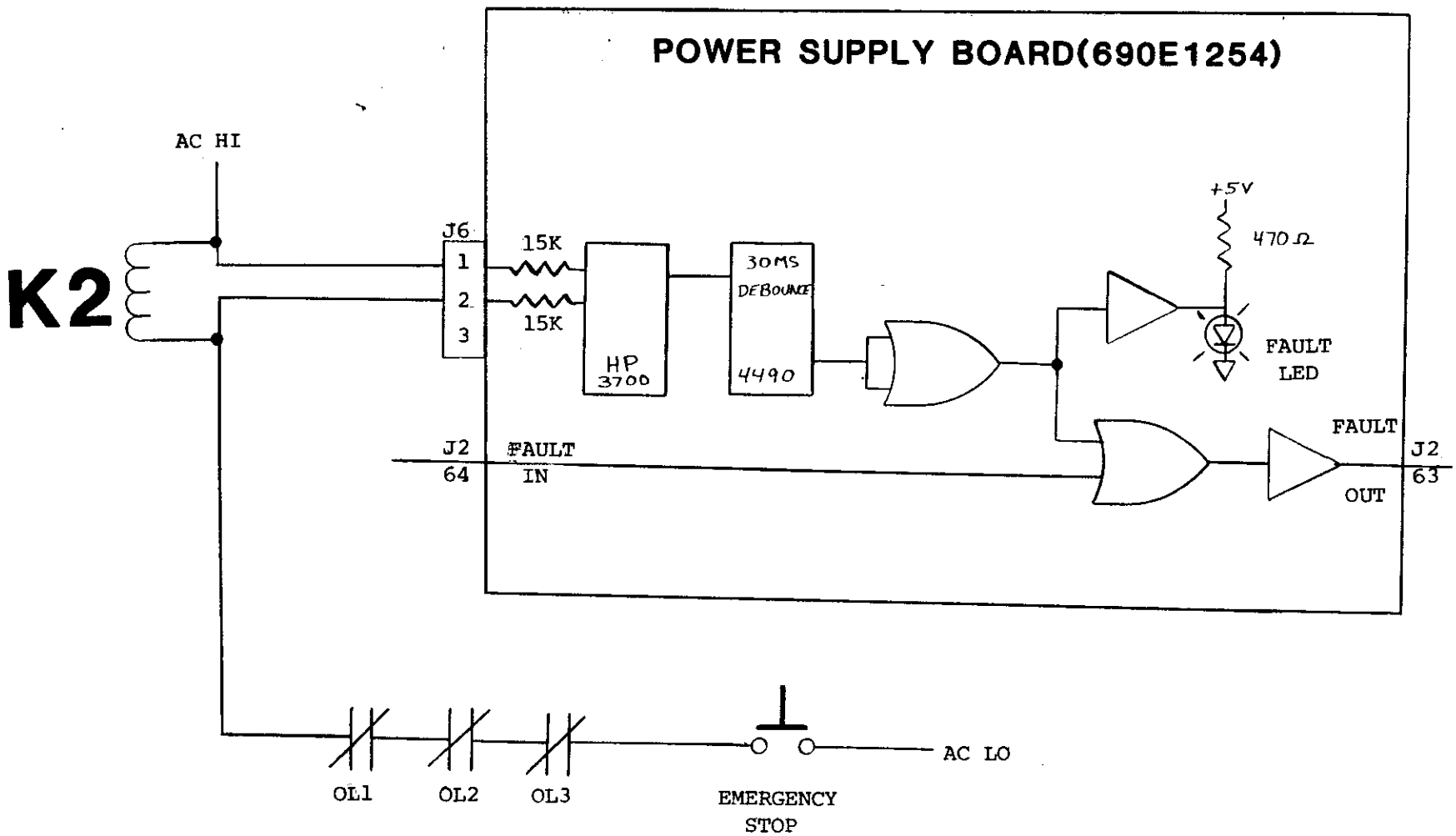




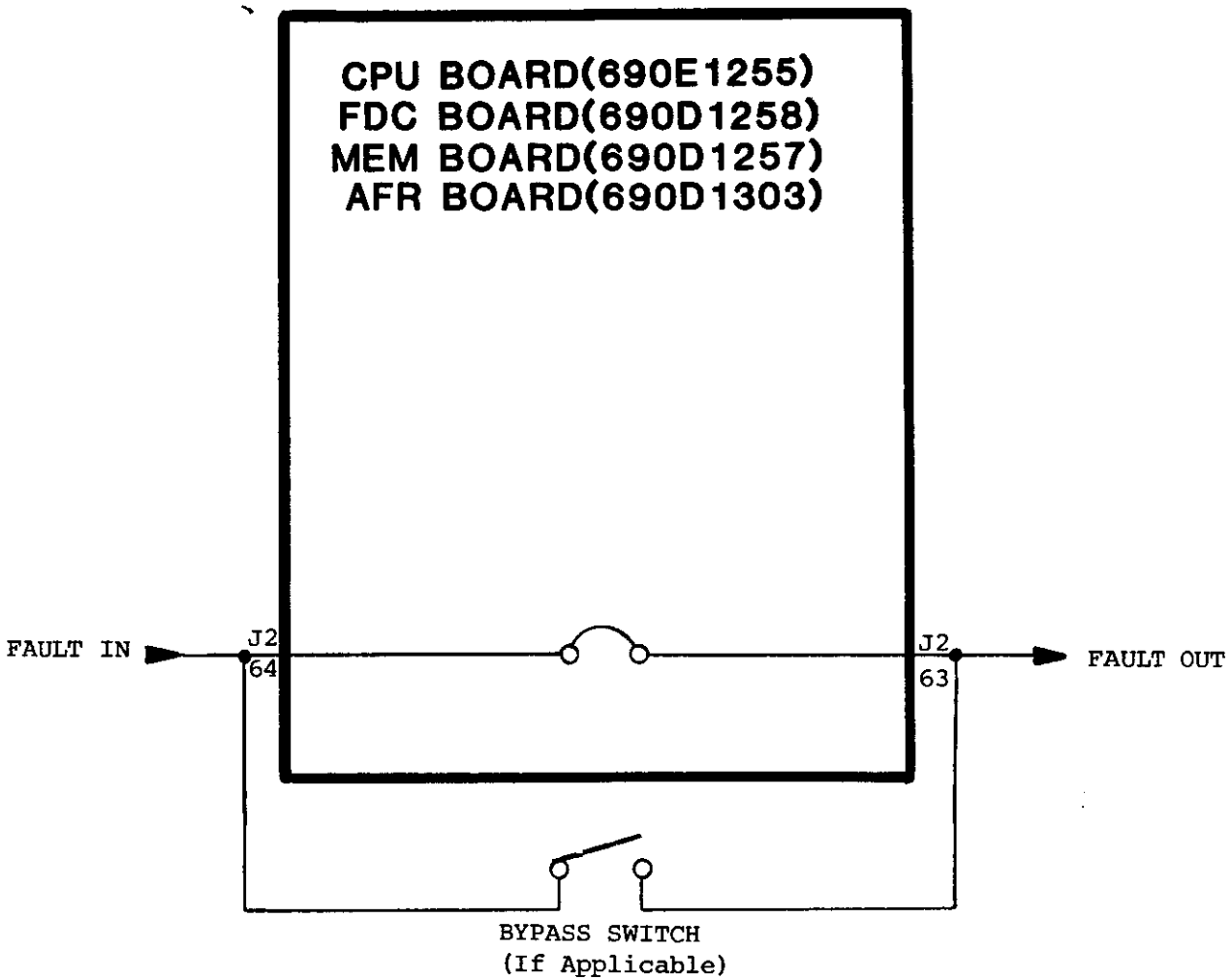
SERVO/INDEXER FAULT CIRCUIT

CRT/LMI FAULT CIRCUIT





POWER SUPPLY FAULT


CPU BOARD(690E1255)
FDC BOARD(690D1258)
MEM BOARD(690D1257)
AFR BOARD(690D1303)
FAULT IN
J2
64
J2
63
FAULT OUT
BYPASS SWITCH
(If Applicable)

POWER SUPPLY BOARD

(690E1254)

SCB OPEN-FRAME SERIES
SWITCHING REGULATED POWER SUPPLIES
OPERATING MANUAL

A. INTRODUCTION

This Operating Manual covers the standard SCB series including the SCB104, SCB134, SCB174, SCB205 and SCB306. Please read it carefully before attempting to use the power supplies.

The SCB Series is particularly designed for use with EDP equipment including main frames and peripherals. They utilize a +5V master circuit in conjunction with 3 to 5 slave circuits. The primary control loop is in the master circuit while the slave circuits are coupled to the master by means of a common output transformer.

The series has over-current protection and overvoltage protection, the latter on the +5V output. They can be used with either 115VAC or 230VAC input power from 47-to-440Hz.

B. SPECIFICATIONS: The following are the specifications for the standard SCB Series.

MODELS	Output No.1 V(nom.)/I(max.)	Output No. 2 V(nom.)/I(max.)	Output No. 3 V(nom.)/I(max.)	Output No. 4 V(nom.)/I(max.)	Output No. 5 V(nom.)/I(max.)	Output No. 6 V(nom.)/I(max.)	Cont. Total Output (Max.)
SCB104-01	+5V/10A	+12V/1.5A	−12V/1.5A	−5V/1.5A			100W
SCB104-02	+5V/10A	+15V/1.5A	−15V/1.5A	−5V/1.5A			
SCB104-03	+5V/10A	+12V/1.5A	−12V/1.5A	+24V/1.5A			
SCB104-04	+5V/10A	+15V/1.5A	−15V/1.5A	+24V/1.5A			
SCB134-01	+5V/10A	+12V/4A	−12V/4A	−5V/2A			130W
SCB134-02	+5V/10A	+15V/4A	−15V/4A	−5V/2A			
SCB134-03	+5V/10A	+12V/4A	−12V/4A	+24V/2A			
SCB134-04	+5V/10A	+15V/4A	−15V/4A	+24V/2A			
SCB174-01	+5V/15A	+12V/4A	−12V/4A	+24V/4A			170W
SCB174-02	+5V/15A	+15V/4A	−15V/4A	+24V/4A			
SCB174-03	+5V/15A	+12V/4A	−12V/4A	−5V/2A			
SCB174-04	+5V/15A	+15V/4A	−15V/4A	−5V/2A			
SCB205-01	+5V/20A	+12V/4A	−12V/4A	−5V/2A	+24V/4A		200W
SCB205-02	+5V/20A	+15V/4A	−15V/4A	−5V/2A	+24V/4A		
SCB205-03	+5V/20A	+12V/4A	−12V/4A	−24V/2A	+24V/4A		
SCB205-04	+5V/20A	+24V/4A	−24V/4A	−12V/2A	+24V/4A		
SCB205-05	+5V/25A	+12V/4A	−12V/4A	−5V/2A	+24V/4A		
SCB306-01	+5V/20A	+12V/4A	−12V/4A	+24V/4A	+15V/4A	−15V/4A	300W
SCB306-02	+5V/20A	+12V/4A	−12V/4A	−5V/1A	+24V/4A	−24V/4A	

OUTPUT SPECIFICATIONS:

Line Regulation (max.): 0.2%

Load Regulation (max.): ...+5V=0.3%; ±12V, ±15V, ±24V = 5%; -5V =6%
(at 20%-100% of max. rated load)

Load Interaction (max):
+5V — any output changed from 50%-100% at max. rated load =0.3%
Other outputs — when +5V output changed from 50%-100% of max. rated load =5%
Other outputs — when any other output excluding +5V is changed from 20%-100% of max. rated load =1%

Output Voltage Adjustment (max.) +5V ....from 4.5V to OVP trip point. VR1
All outputs when +5V is set at 5.00V (centering) = ±5%

Overvoltage Protection: +5V Output ..... 6.5V ±0.5V

Overload Protection:

Maximum current cannot be drawn from all outputs at the same time. At no time should the average power rating be exceeded. Above the maximum power rating the overload protection feature will reduce all output voltages to a safe dissipation level. The overload feature will also protect against short circuits on any single line.

INPUT SPECIFICATIONS:

Input Voltages: 115/230VAC
(-20% to +10%=90-127VAC & 180-254VAC

Frequency Range: 47-440Hz

Inrush Current: ..... 25A max. peak cold start

Hold-Up Time (min.): .... 15mS at full-load and nominal input voltage

Fuse on Input Line

GENERAL SPECIFICATIONS:

Full Output Rating ..... to 50°C (derated to 50% at 70°C)

Minimum Load: ..... 20% of full load

Ambient Temperature Range:
Operating ..... 0 to +70°C
Storage ..... -20 to +85°C

Temperature Coefficients (typ.) ..... +5V=0.02%/°C
other outputs=0.05%/°C

Efficiency (typ.) 75%

Noise and Ripple — PARD: ..... Peak-to-peak (typ.) = 2%
RMS (max.) = 40mV

Dielectric Withstand:
Input/output & Input/Gnd. =1, 500VAC for 1 minute
Output-to-Gnd. = 500VAC for 1 minute

Cooling: ..... Convection

KEC ELECTRONICS, INC.
20817 Western Avenue, Torrance, California 90501 • Phone (213) 320-3902 • TWX 910-349-6962

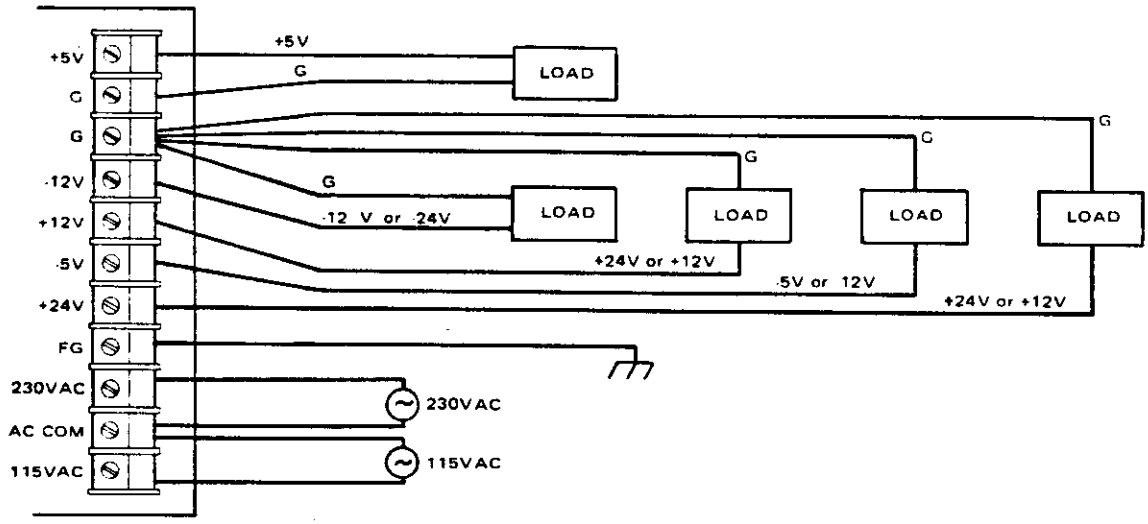
C. INSTALLATION

The single barrier strip provides input-output terminations for the power supply. The diagram below shows generally how to connect to the barrier strip. All G terminals are Output-Common returns, while FG is a Frame-Ground termination. On the SCB306, two outputs have isolated returns, which can be connected in common if desired. AC input power is connected between AC Common and either 115VAC or 230VAC. On the SCB306 a jumper wire on the PC board must be connected to the 115 or 230 position for proper input voltage operation with the two AC input terminals available on the barrier strip.

The units can be mounted in any position by means of 8 - 32 tapped holes on the bottom and side of the L bracket to which the power supply is fastened. For full ratings the unit should attach to a metal surface and should be used in a moving air environment. The SCB306 tapped holes are 6 -32 (5).

For information on the outline dimensions and installation, please refer to the back page.

BARRIER STRIP CONNECTION DIAGRAM



D. OPERATION

Since this unit is designed with a master/slave control configuration, adjustment of the +5V master also controls all of the slave outputs. Load changes of the master affect the slave circuits and load changes in the slave outputs have some effect on the other slaves and the master. Please refer to the cross regulation specification for details.

In order for the system to operate within the specifications, there must be a 20% minimum load on all outputs. Failure to do so in the case of the master circuit will result in extremely poor functioning of the slave outputs. However, a no load condition on a slave circuit will only cause its output voltage to rise to approximately 15% above the normal rating.

Output Voltage Setting

The +5V master output can be set in the range of +4.5V to the OVP trip-point by means of VR1. Turning VR1 clockwise will increase the output voltage. During normal operation the red LED located near the terminal strip will be ON.

When the output voltage is adjusted by means of VR1, all output voltages are changed proportionally. For proper operation, the +5V master output should be adjusted within a ±10% band. The VR1 potentiometer is located on the main PC Board on all models, with the exception of the SCB 306, where it is mounted on one of the vertical Control Circuit PC cards.

Maximum Output Rating

Each output has its own maximum available current rating as shown in the specification table, however, all maximum output currents cannot be drawn simultaneously. In any case, the maximum output dissipation rating cannot be exceeded.

For pulse loads both of these ratings must be taken into consideration.

Overvoltage Protection (OVP)

The overvoltage protection (OVP) setting is factory adjusted at 6.5V ±0.5V. The actual set point can be verified by adjustment of VR1 (clockwise to increase). When making this check be sure that the power supply is operating under load.

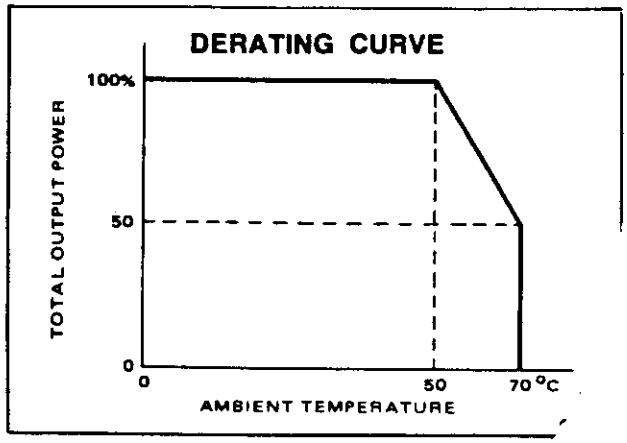
When the OVP voltage level is reached, the power supply will shut down. At this point the LED will be turned off.

In order to restart, the condition causing the OVP to trigger should be removed. Then the AC line switch should be turned off, and then turned on again, and the unit will operate.

Cooling

The SCB series is intended for use in a moving air environment. For derating information, refer to the curve shown below.

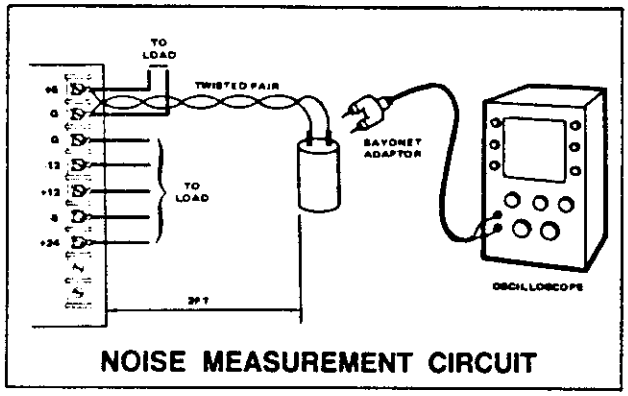
When used in a convection cooled environment, be sure that the power supply is attached to a metal chassis.



Output Noise and Ripple

The Switching Regulated Power Supply requires some additional care in reducing noise such as the use of twisted pairs and the use of adequate decoupling capacitors.

For noise measurements, the following standard method is suggested for approximating actual use. In order to avoid ground loops, the oscilloscope should be connected to the power line through an isolation transformer.



NOISE MEASUREMENT CIRCUIT

Overcurrent Protection (OCP)

Overcurrent protection is provided by Fold-Back circuitry based on total output. When the total output exceeds approximately 115% of its rating, the OCP circuit will operate, decreasing the output voltages. As the overload condition is reduced, the output voltage levels will automatically be restored.

As the power supply goes into overload, the red LED will begin to flash, and when the output drops approximately 10%, it will extinguish.

The OCP setting is made at the factory by means of VR2 and should not be reset.

For checking the OCP function, bring the +5V master output to full-load and all of the slave circuits close to their full-load rating, taking care not to exceed the total power dissipation rating of the supply. OCP operation can then be observed by shorting or overloading one of the outputs. Be sure to have a load on each output when conducting this test.

AC Power Fail Signal

AC Power Fail is available as an option on the SCB series. The power fail signal is available at either the output terminal strip marked ACPF, or from a Molex connector.

Under normal operating conditions there is a +5V signal between ACPF and G. If the AC input power is removed, the signal will drop to OV, 5ms after the removal of AC input power. The power fail signal will also drop to OV of there is no output voltage for any reason.

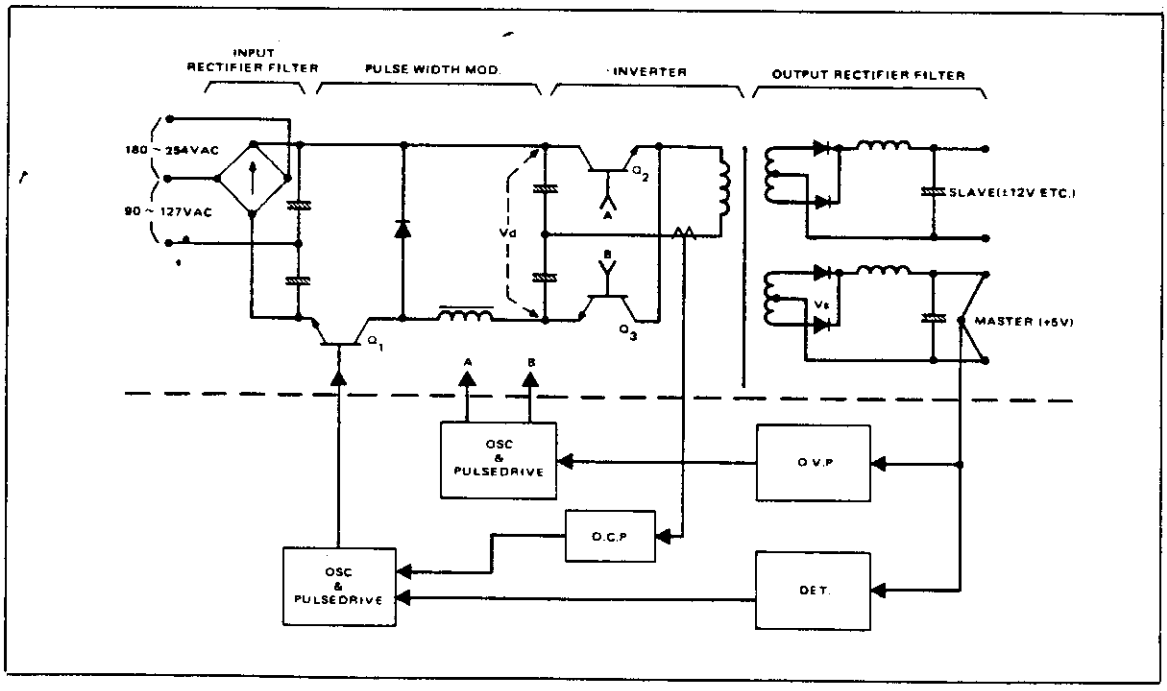
The Power Fail modules are designed for use with either 115 VAC or 230 VAC inputs, and will provide the same output signal regardless of which voltage is connected to the AC input terminals.

E. THEORY OF OPERATION

The SCB series consists of an input rectifier, pulse-width modulator (Q_1), push-pull inverter (Q_2, Q_3) and output rectifier circuits. The control loop is in the +5V master output circuit.

In the circuit diagram, voltage (V_d) is controlled by the pulse-width modulator (Q_1) which derives its error signals from the +5V (V_d) is corrected, since all output voltages derive from a common output transformer.

The overvoltage protection circuit stops the pulse driver to the inverter which cuts off all outputs. The overload protection circuit consists of a current transformer in the primary line set to total output and cuts off the pulse width modulator if the preset level is exceeded.



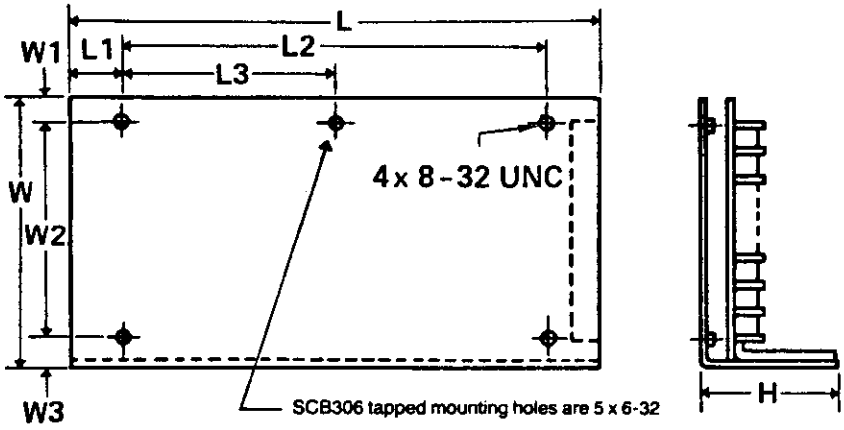
ıut. The secondary output voltage (V_S) is in turn determined by . As the +5V line is loaded, (V_S) increases to maintain a ıtant output, increasing the output voltage on the slave ıts. This is the effect of cross-regulation.

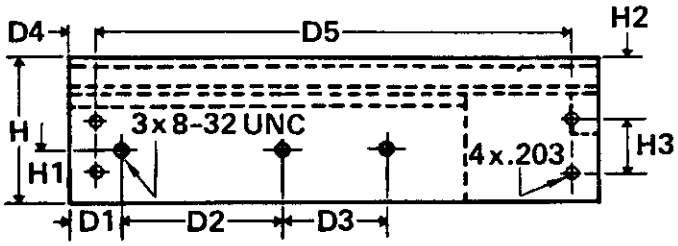
the load on the slave circuits changes, (V_S) changes and

There is additional built-in protection. If the pulse width modulator (Q_1) is shorted, then the overvoltage protection circuit will trigger and stop the pulse drivers. If (Q_2) or (Q_3) shorts, then the overload protection circuit is triggered which stops the pulse-width modulator. There is also a built-in line fuse on the input.

F. INSTALLATION DIAGRAMS

Outline Drawings





Dimensions Table

DIM.	MODEL NUMBERS				
	SCB104	SCB134	SCB174	SCB205	SCB306
H	2.44/62	2.44/62	2.44/62	2.44/62	2.50/64
L	9.06/230	11.0/279	10.0/254	13.0/330	11.75/298
W	4.13/105	4.94/125.5	5.63/143	4.94/125.5	7.60/193
H1	0.9/23	0.9/23	0.9/23	0.9/23	
H2					1.00/25.5
H3					1.25/32
L1	1.18/30	0.26/6.5	0.39/10	1.67/42.5	0.26/6.5
L2	7.09/180	7.68/195	8.23/209	9.84/250	5.25/133
L3					10.50/266.7
W1	0.39/10	0.39/10	0.39/10	0.39/10	
W2	3.35/85	3.94/100	4.57/116	3.98/101	7.00/177.5
W3					0.38/9.5
D1	1.87/47.6	1.14/29	1.14/29	1.50/38	
D2	4.82/122.5	2.99/76	2.99/76	5.00/127	
D3		1.38/35	1.38/35	5.00/127	
D4					0.38/9.5
D5					11.00/279
WHT.	2.42/1.10	2.77/1.26	2.86/1.30	3.74/1.70	4.75/2.15

Note: Inches or lbs./mm or kilograms.

WARRANTEE

KEC SCB Series Switching Regulated Power Supplies are warranteed to be free from defects in material or workmanship for 2 years from the date of invoice. Units will be repaired free of charge if they are returned to KEC, with return postage prepaid, and with return authorization from KEC or its representatives. This offer does not apply to units which have been altered or damaged by misuse or handling. This warrantee is in lieu of any other warrantees expressed or implied.

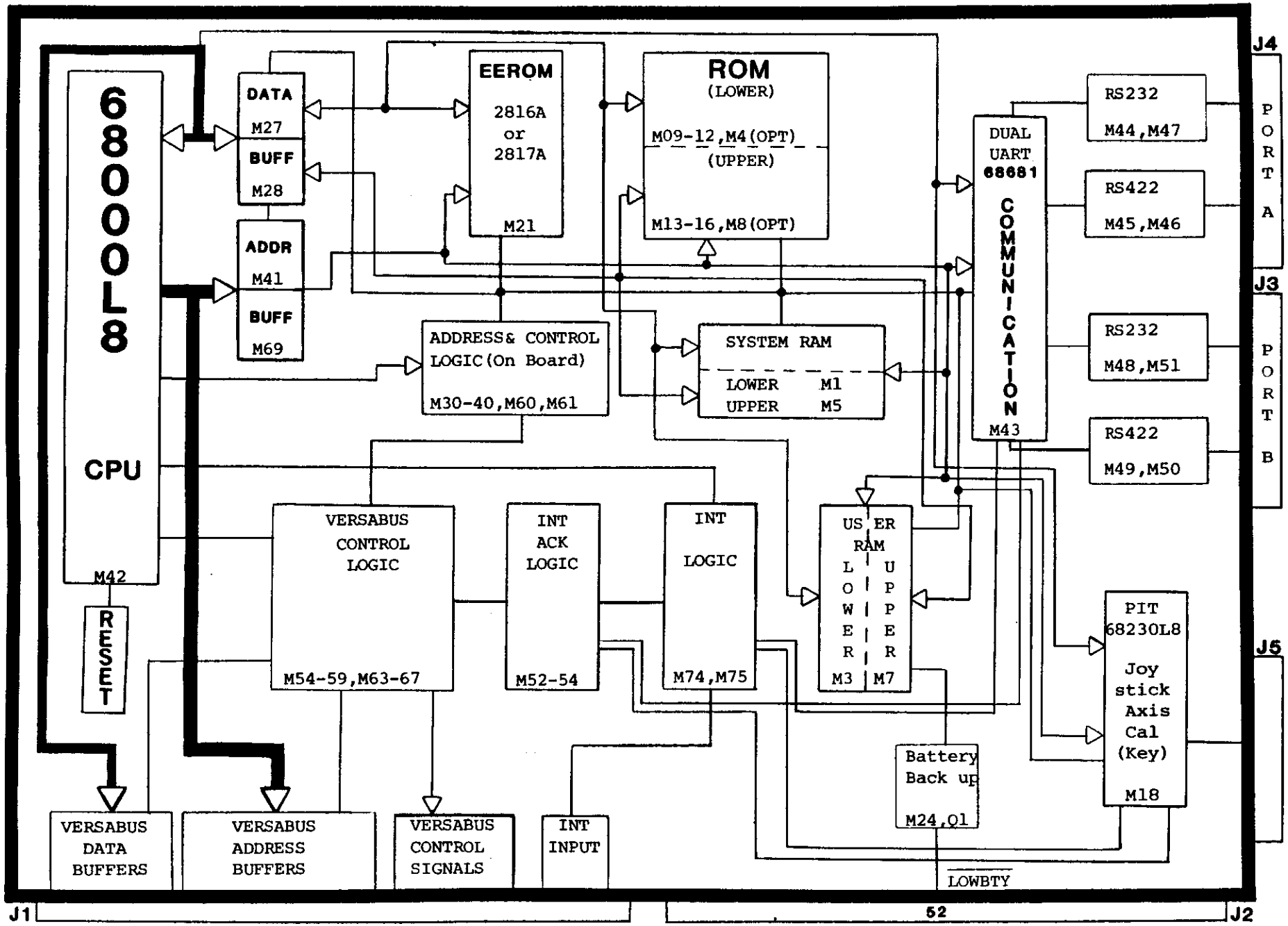
KEC ELECTRONICS, INC.

20817 Western Avenue, Torrance, California 90501 • Phone (213) 320-3902 • TWX 910-349-6

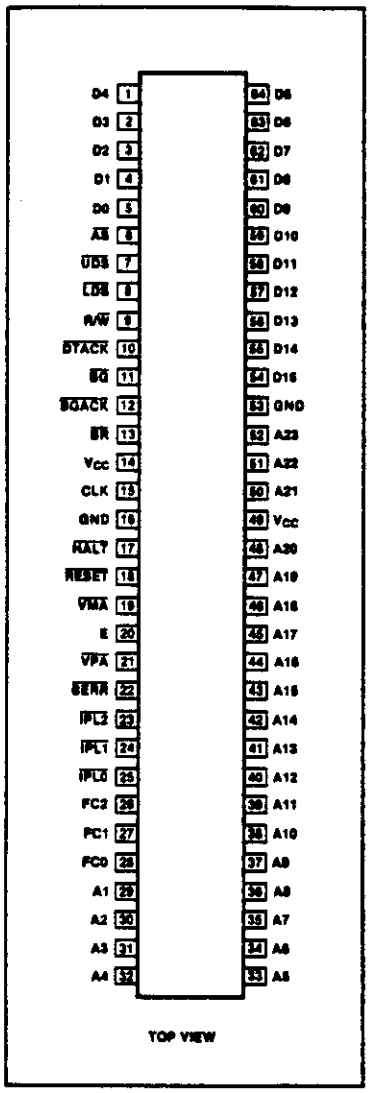
CPU BOARD

(690E1255)

BLOCK DIAGRAM- CPU BOARD



PIN CONFIGURATION[1]



1

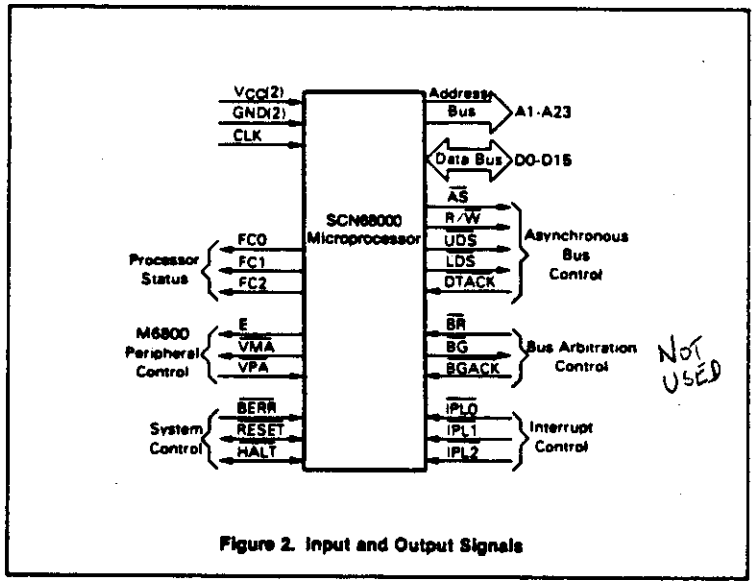


Figure 2. Input and Output Signals

2

Table 1 SIGNAL SUMMARY

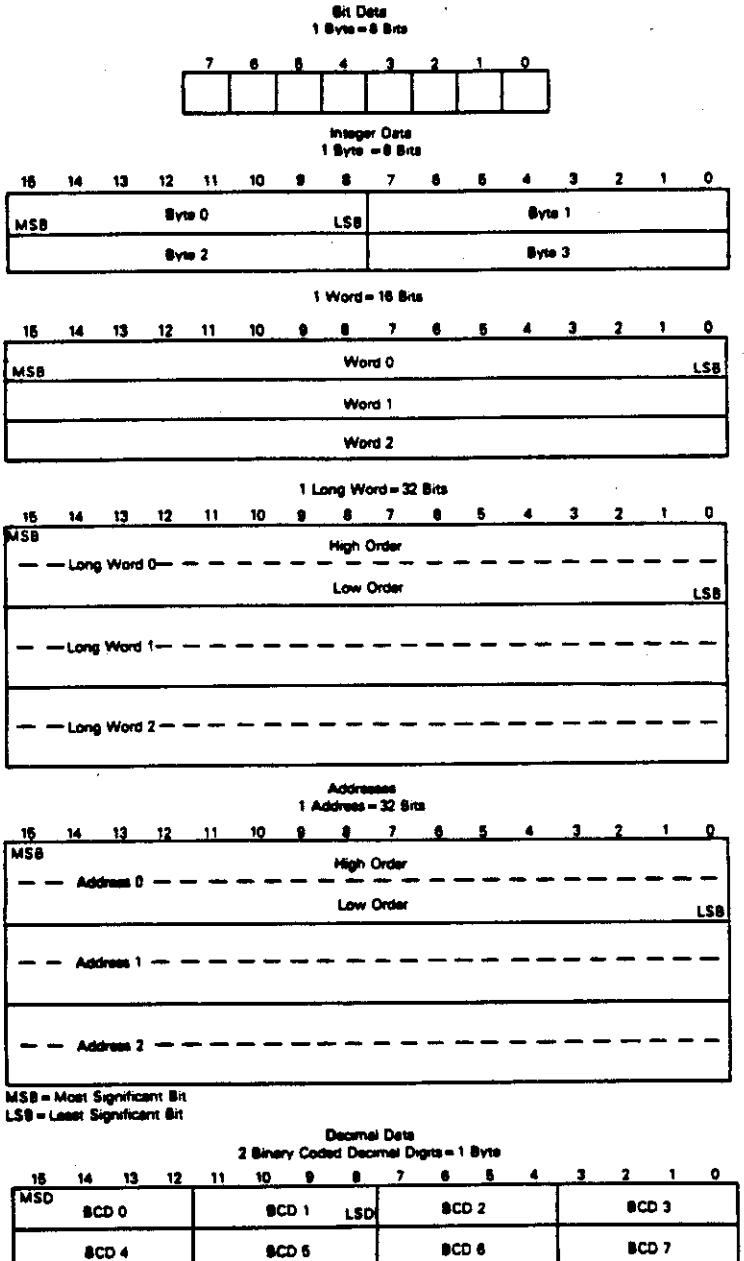
Signal Name	Mnemonic	Input/Output	Active State	Three State
Address Bus	A1-A23	output	high	yes
Data Bus	D0-D15	input/output	high	yes
Address Strobe	$\overline{AS}$	output	low	yes
Read/Write	R/$\overline{W}$	output	read-high write-low	yes
Upper and Lower Data Strobes	$\overline{UDS}$, $\overline{LDS}$	output	low	yes
Data Transfer Acknowledge	$\overline{DTACK}$	input	low	—
Bus Request	$\overline{BR}$	input	low	—
Bus Grant	$\overline{BG}$	output	low	no
Bus Grant Acknowledge	$\overline{BGACK}$	input	low	—
Interrupt Priority Level	$\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$	input	low	—
Bus Error	$\overline{BERR}$	input	low	—
Reset	$\overline{RESET}$	input/output	low	no*
Halt	$\overline{HALT}$	input/output	low	no*
Enable	E	output	high	—
Valid Memory Address	$\overline{VMA}$	output	low	yes
Valid Peripheral Address	$\overline{VPA}$	input	low	—
Function Code Output	FC0, FC1, FC2	output	high	yes
Clock	CLK	input	high	no
Power Input	V_{CC}	input	—	—
Ground	GND	input	—	—

*open drain

Table 2 DATA STROBE CONTROL OF DATA BUS

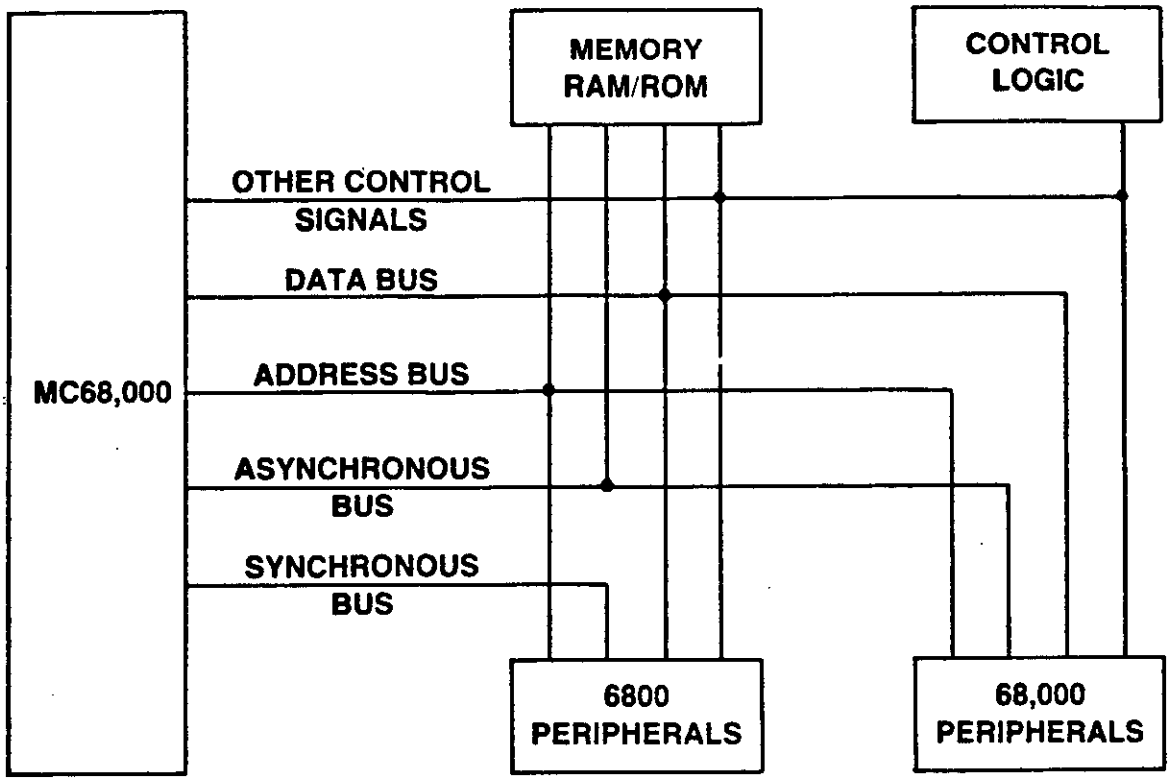
$\overline{UDS}$	$\overline{LDS}$	R/$\overline{W}$	D8-D15	D0-D7
High	High	—	No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7*	Valid data bits 0-7
Low	High	Low	Valid data bits 8-15	Valid data bits 8-15*

*These conditions are a result of current implementation and may not appear on future devices.



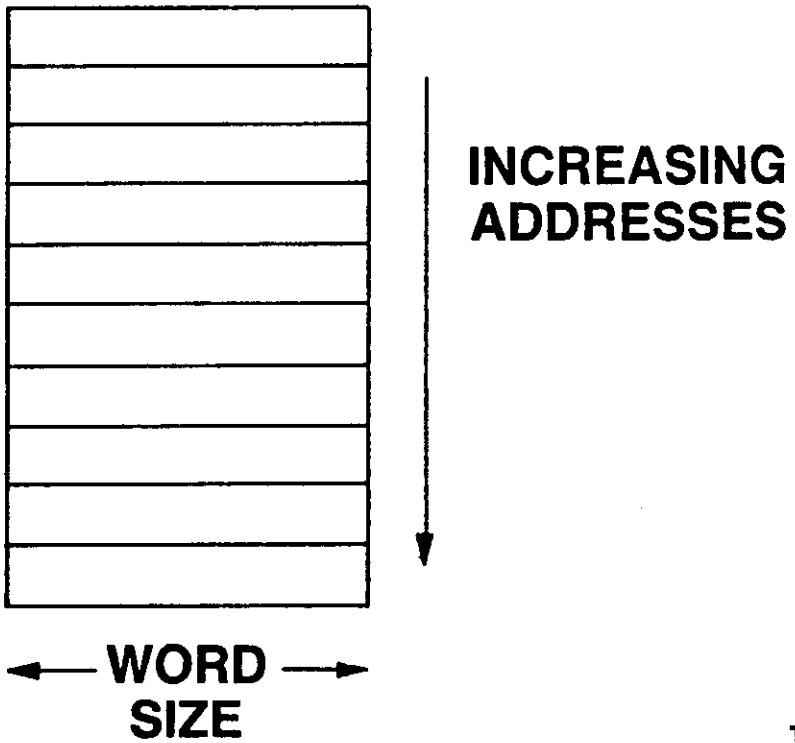
Data Organization in Memory

MC68,000 — BASIC SYSTEM DIAGRAM



TT60

MC68,000 — MEMORY DIAGRAMS



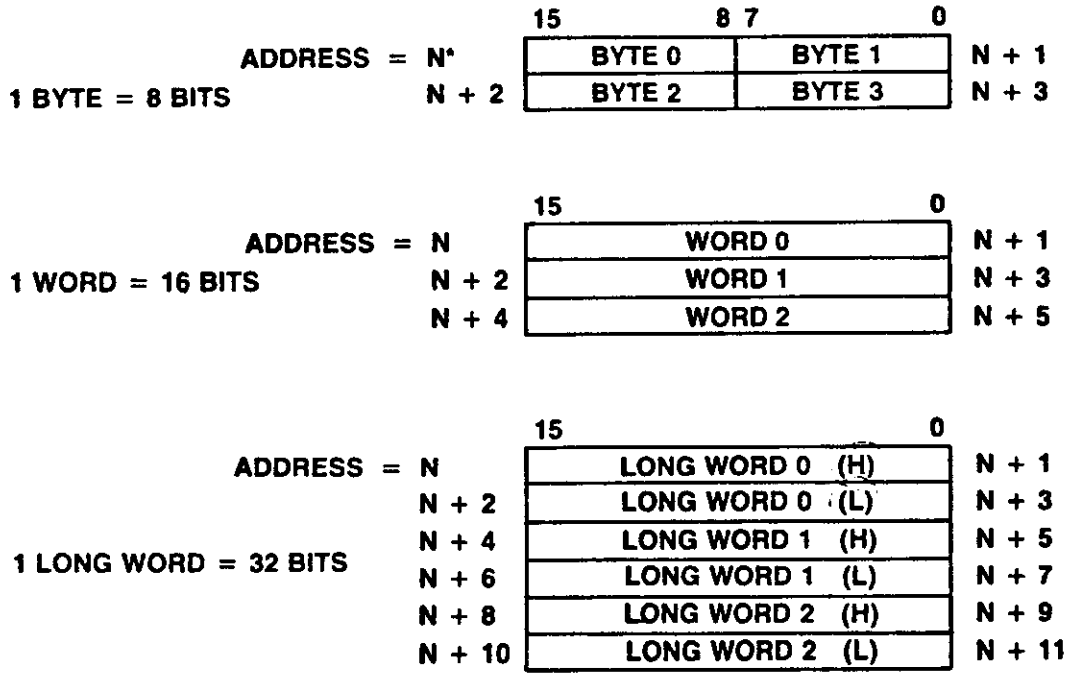
TT159-1

MC68,000 — RULES FOR ACCESSING MEMORY

- WORDS AND LONG WORDS MUST BE ACCESSED FROM AN EVEN ADDRESS.
- BYTES CAN BE ACCESSED FROM EITHER AN ODD OR EVEN ADDRESS.
- OP WORDS MUST BE ON EVEN ADDRESSES.

TT160

MC68,000 INTEGER DATA MEMORY FORMATS



*N IS AN EVEN NUMBER

TT4-3

MC68,000 — CYCLE TIME DEFINITIONS

CLOCK CYCLE

THE INPUT CLOCK PERIOD FROM POSITIVE EDGE TO POSITIVE EDGE

BUS CYCLE

THE SEQUENCE OF TIMING EVENTS REQUIRED TO DO A BYTE OR A WORD READ CYCLE, A BYTE OR A WORD WRITE CYCLE, OR A READ/MODIFY/WRITE CYCLE

INSTRUCTION CYCLE

THE SEQUENCE OF TIMING EVENTS REQUIRED TO DO AN INSTRUCTION

TT158

ASSERTION (ASSERT)

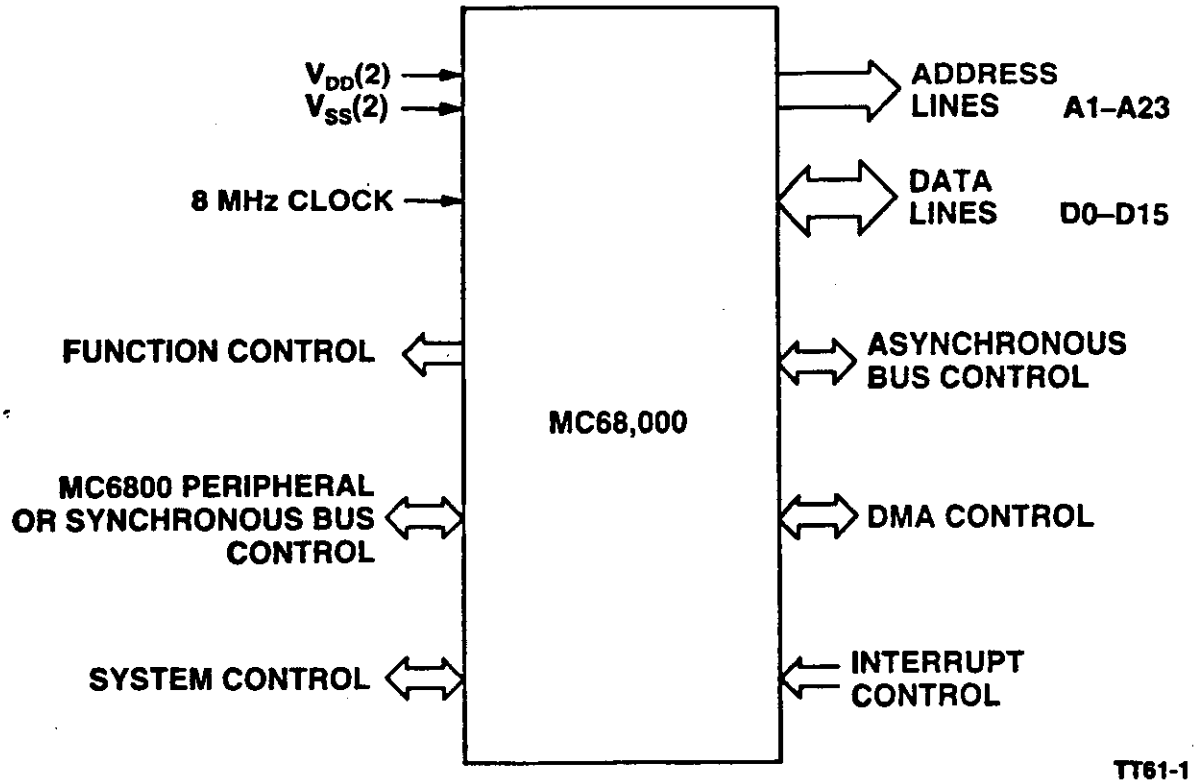
A SIGNAL (PIN) IS ACTIVE OR TRUE INDEPENDENT OF THE ACTUAL VOLTAGE LEVEL.

NEGATION (NEGATE)

A SIGNAL (PIN) IS INACTIVE OR FALSE INDEPENDENT OF THE ACTUAL VOLTAGE LEVEL.

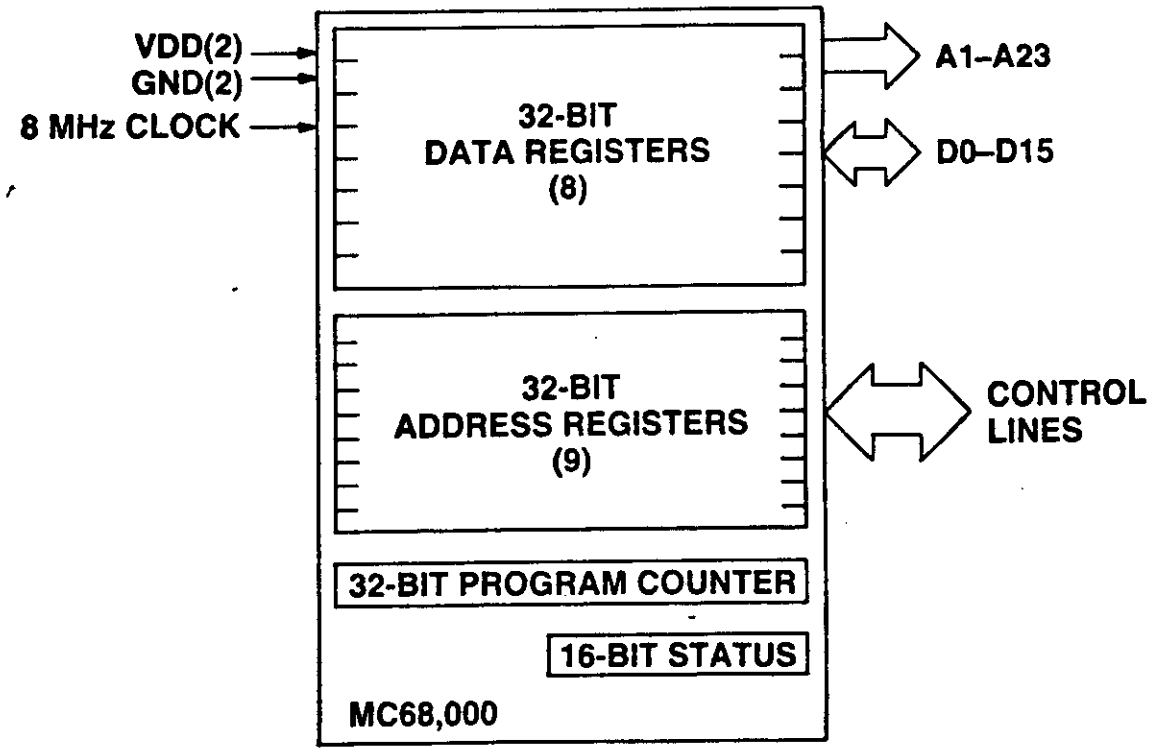
TT1525

MC68,000 — BASIC PIN DIAGRAM



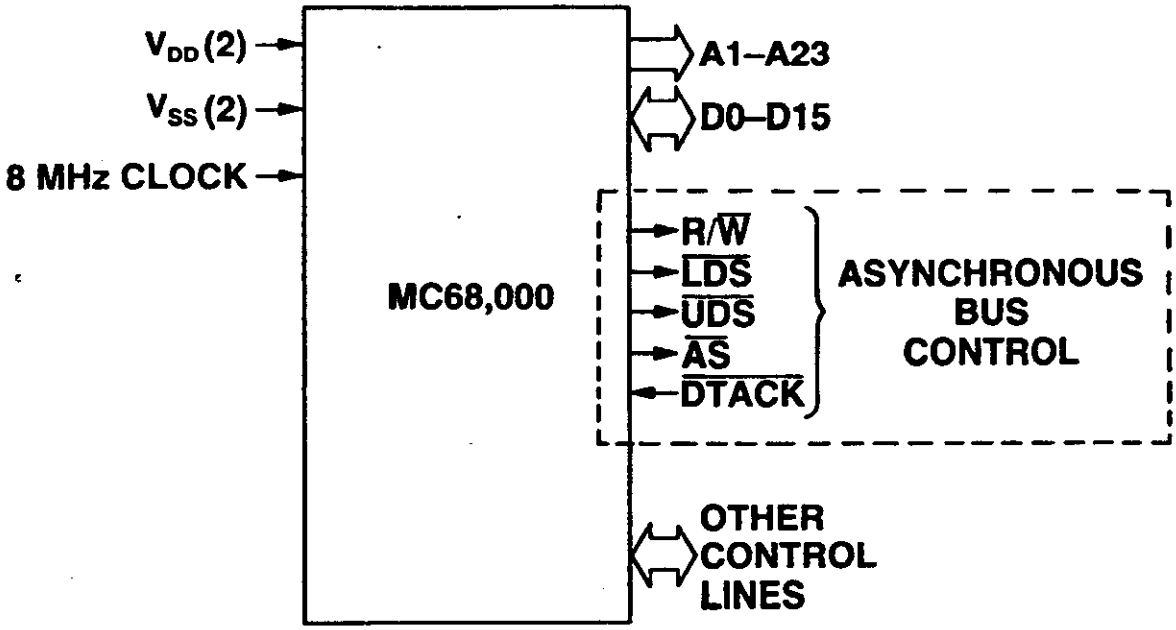
TT61-1

MC68,000 — REGISTER DIAGRAM



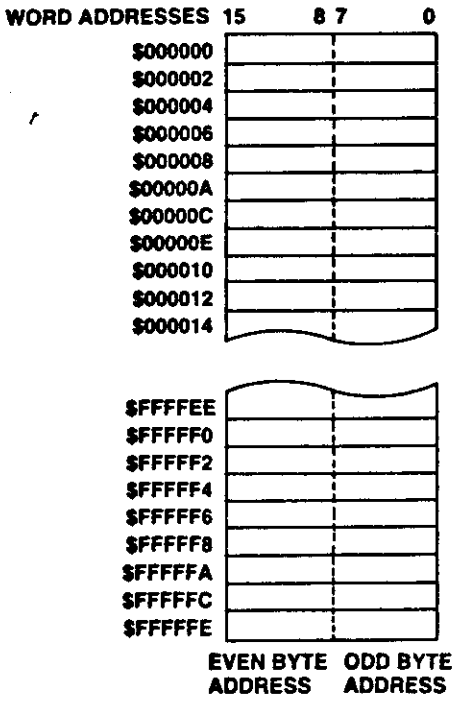
TT62-1

MC68,000 — ASYNCHRONOUS BUS CONTROL DIAGRAM



TT67-1

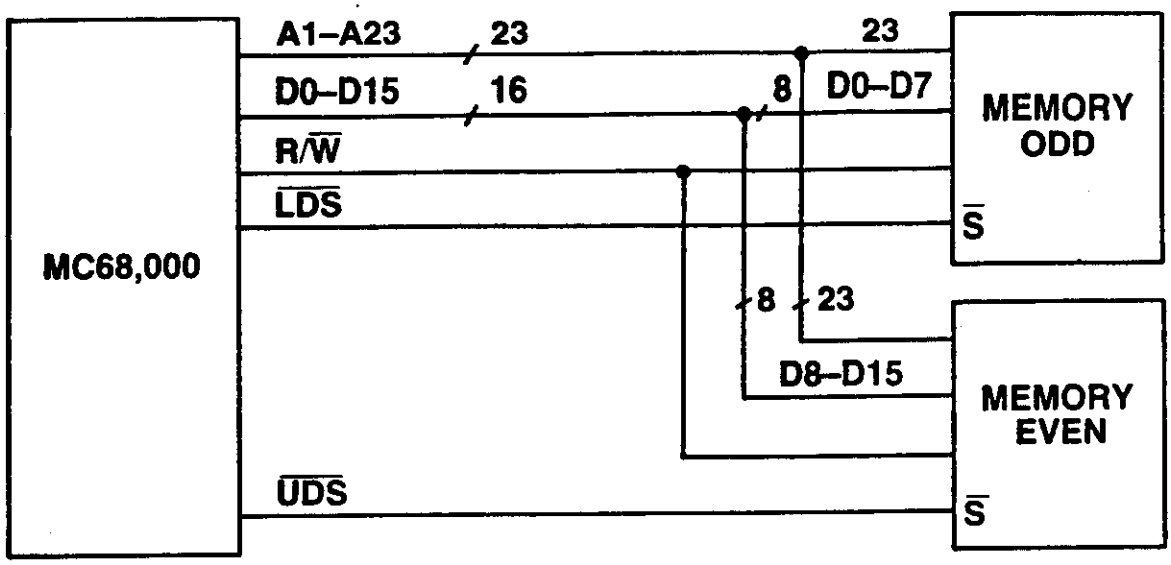
MC68,000 — MEMORY MAP



- TO ACCESS AN EVEN BYTE ADDRESS, A0 = 0, $\overline{UDS}$ = 0, AND $\overline{LDS}$ = 1.
- TO ACCESS AN ODD BYTE ADDRESS, A0 = 1, $\overline{UDS}$ = 1, AND $\overline{LDS}$ = 0
- TO ACCESS A WORD ADDRESS A0 = 0, $\overline{UDS}$ = 0, and $\overline{LDS}$ = 0

TT9-3

MC68,000 — BYTE ADDRESSING



TT10

MC68,000 — BYTE CONTROL

UDS	LDS	R/W	D8–D15	D0–D7
0	0	0	VALID WRITE DATA	VALID WRITE DATA
0	0	1	VALID READ DATA	VALID READ DATA
0	1	0	VALID WRITE DATA	*SAME AS D8–D15
0	1	1	VALID READ DATA	INVALID DATA
1	0	0	*SAME AS D0–D7	VALID WRITE DATA
1	0	1	INVALID DATA	VALID READ DATA
1	1	0	INVALID DATA	INVALID DATA
1	1	1	INVALID DATA	INVALID DATA

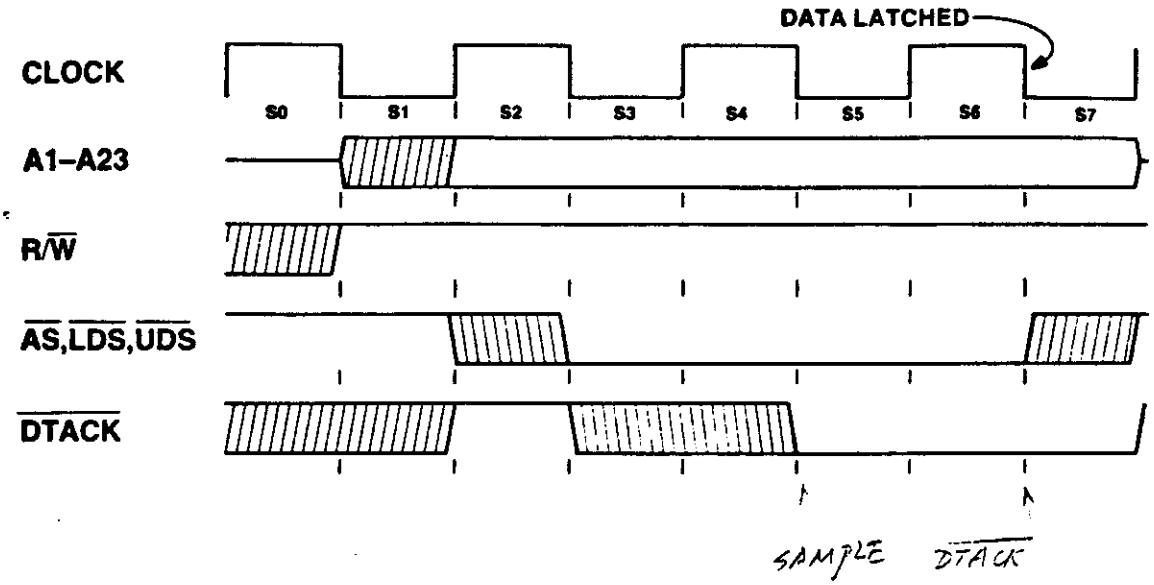
* THIS FEATURE IS NOT PART OF THE 68,000 SPECIFICATION, AND IS NOT ASSURED IN FUTURE VERSIONS.

TT11

SEMI - ASYNCHRONOUS BUS

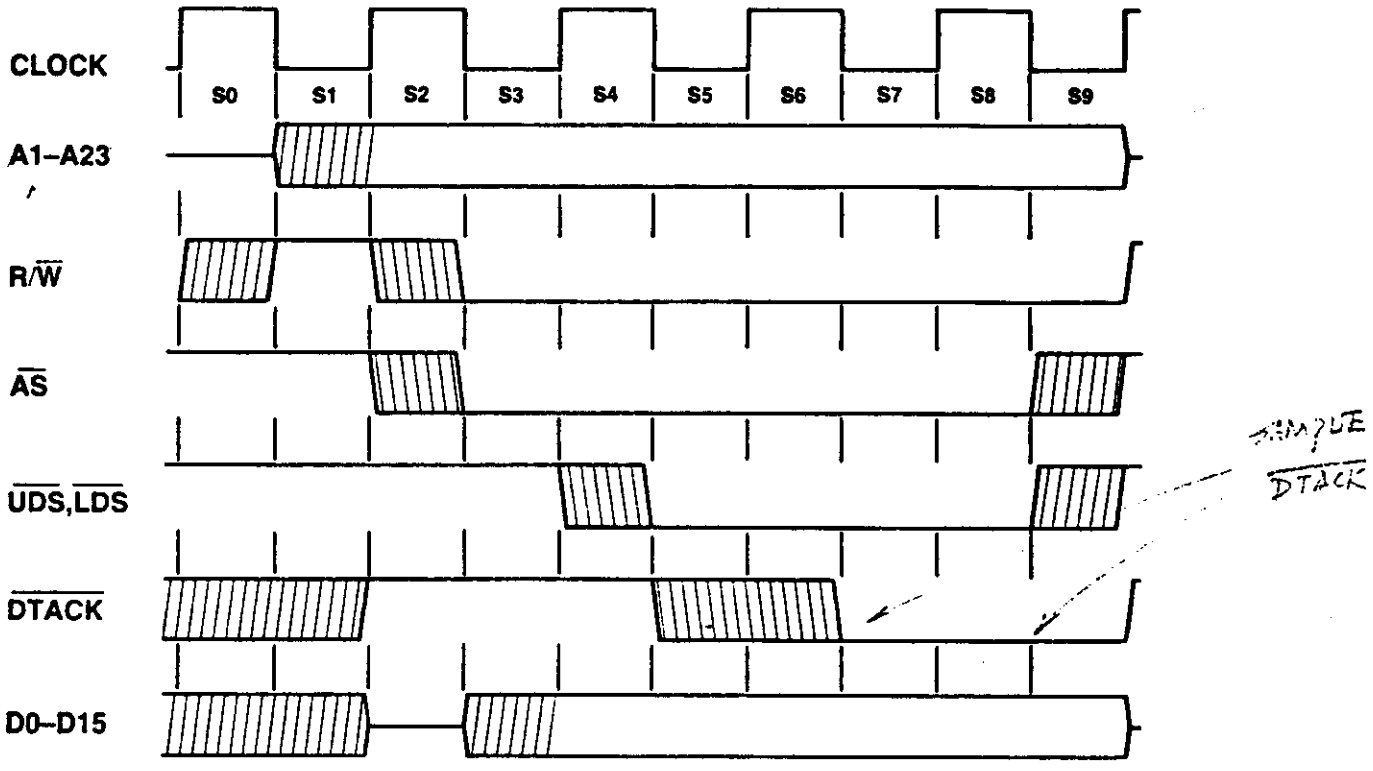
WAIT STATE = n x 2 STATES

MC68,000 READ BUS CYCLE OPERATION (WORD)



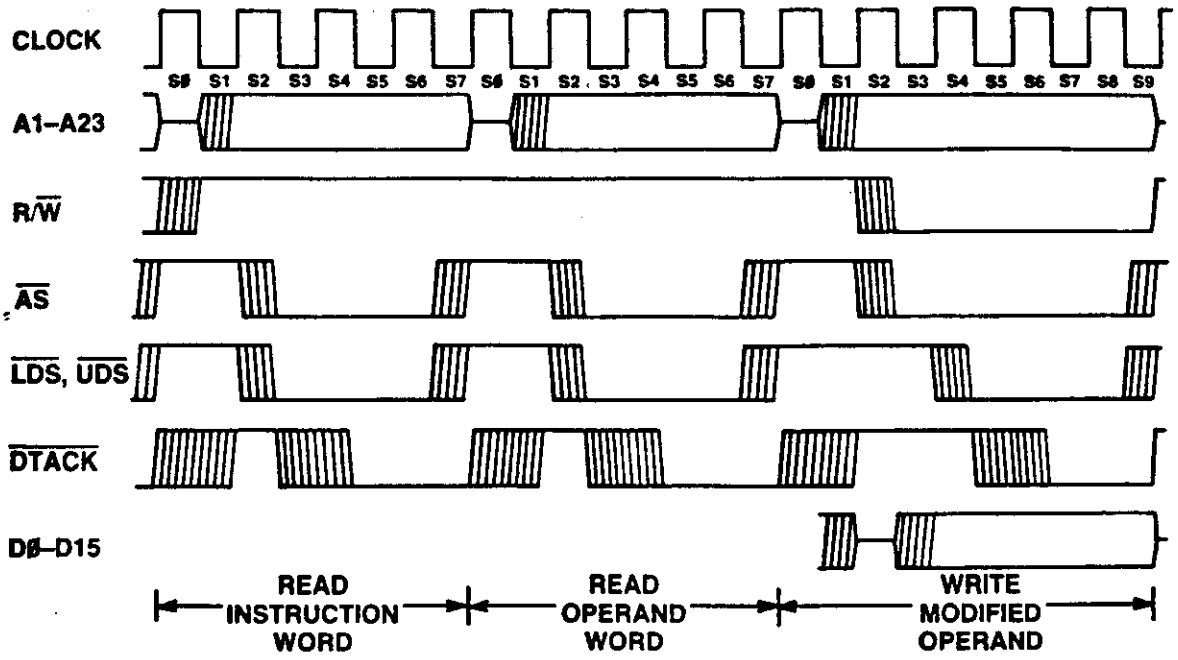
TT12-2

MC68,000 WRITE BUS CYCLE OPERATION (WORD)



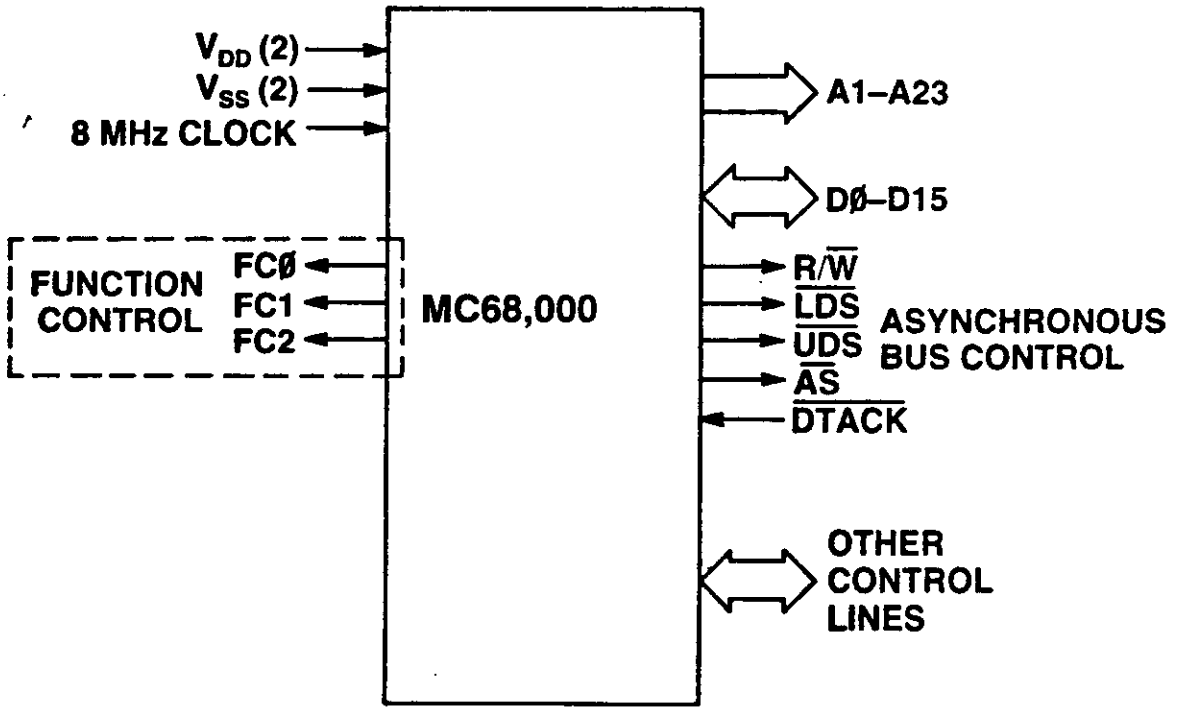
TT13-1

MC68,000 — READ/MODIFY/WRITE INSTRUCTION (WORD)



TT68

MC68,000 — FUNCTION CONTROL PIN DIAGRAM



TT69-1

MC68,000 — FUNCTION CONTROL STATES

FC2	FC1	FC0	STATE	MODE
0	0	0	RESERVED	USER
0	0	1	DATA SPACE	USER
0	1	0	PROGRAM SPACE	USER
0	1	1	RESERVED	USER
1	0	0	RESERVED	SUPERVISOR
1	0	1	DATA SPACE	SUPERVISOR
1	1	0	PROGRAM SPACE	SUPERVISOR
1	1	1	INTERRUPT ACKNOWLEDGE	SUPERVISOR

TT15-1

MC68,000 — PROGRAM VS. DATA

THE FUNCTION CONTROL OUTPUTS INDICATE PROGRAM WHEN:

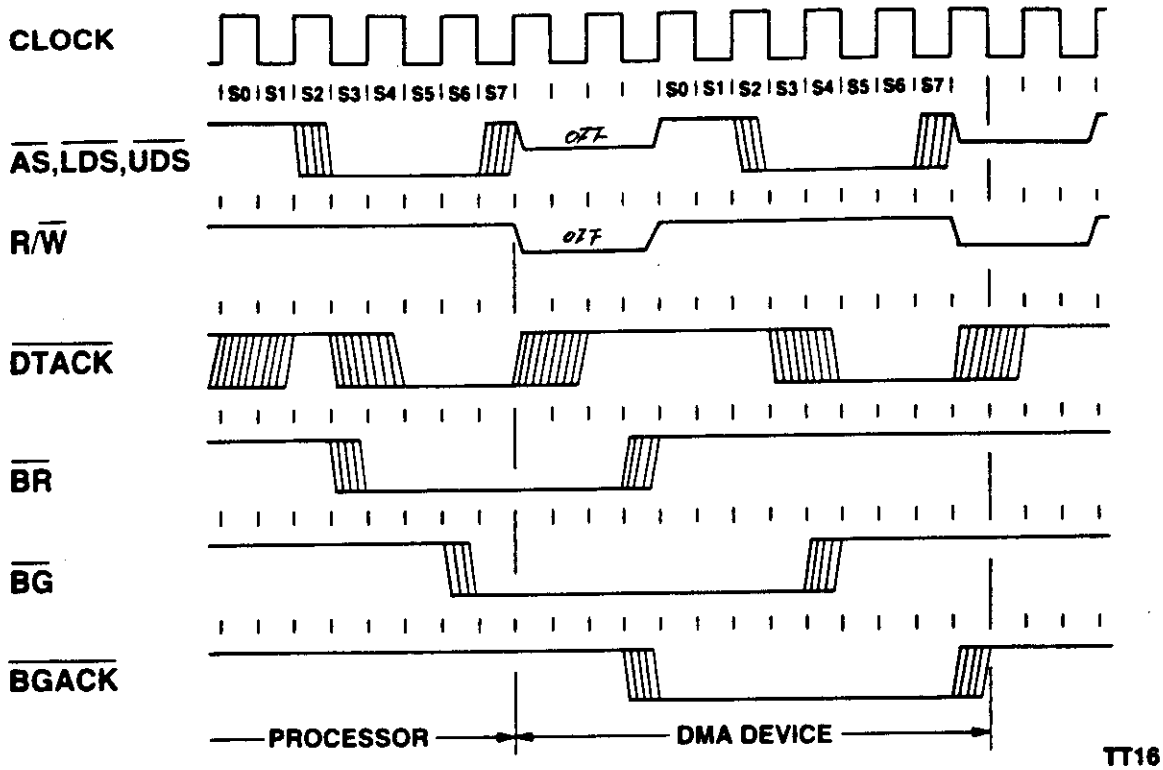
- PC IS THE ADDRESS SOURCE
- RESET VECTORS ARE FETCHED

THE FUNCTION CONTROL OUTPUTS INDICATE DATA WHEN:

- MOST OPERANDS ARE READ (PC IS NOT ADDRESS SOURCE)
- ALL OPERANDS ARE WRITTEN
- VECTORS OTHER THAN RESET ARE FETCHED

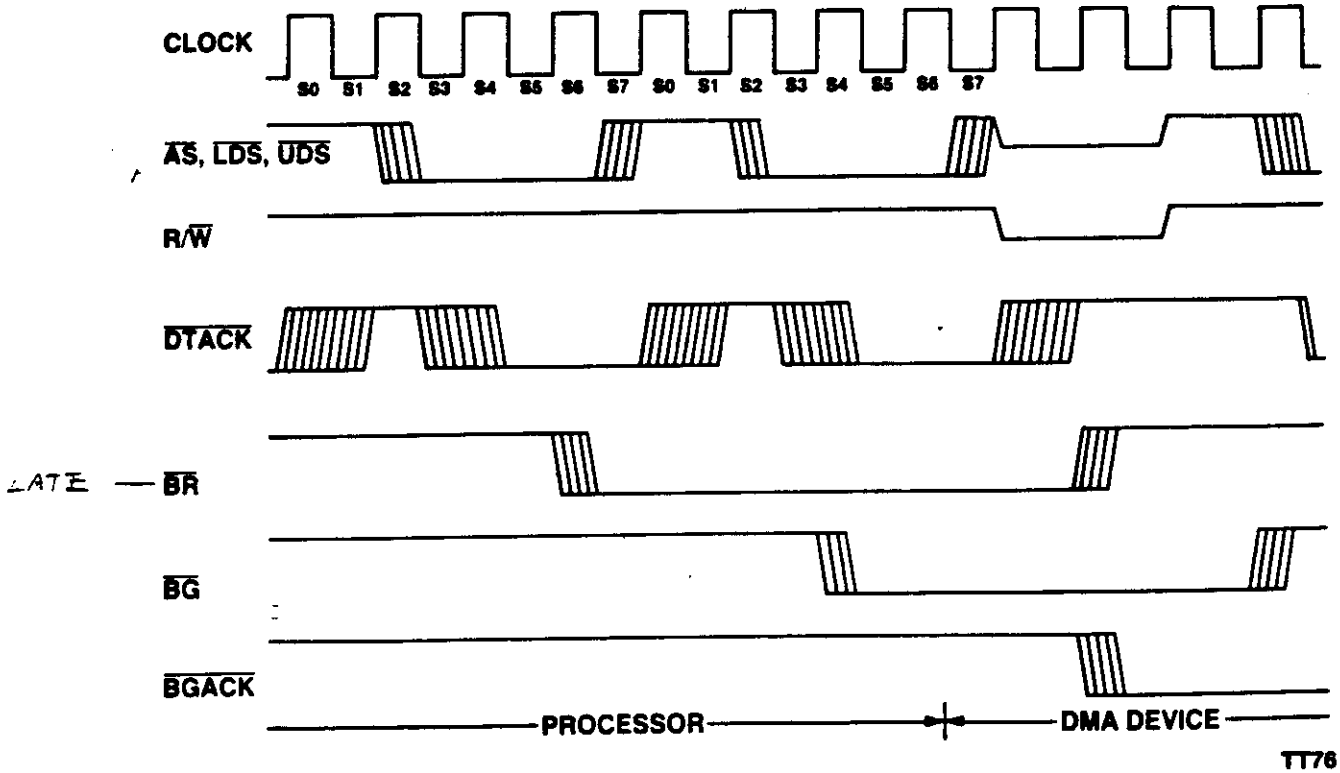
TT156-2

MC68,000 — BUS REQUEST TIMING



TT16

MC68,000 — BUS REQUEST TIMING DIAGRAM



TT76

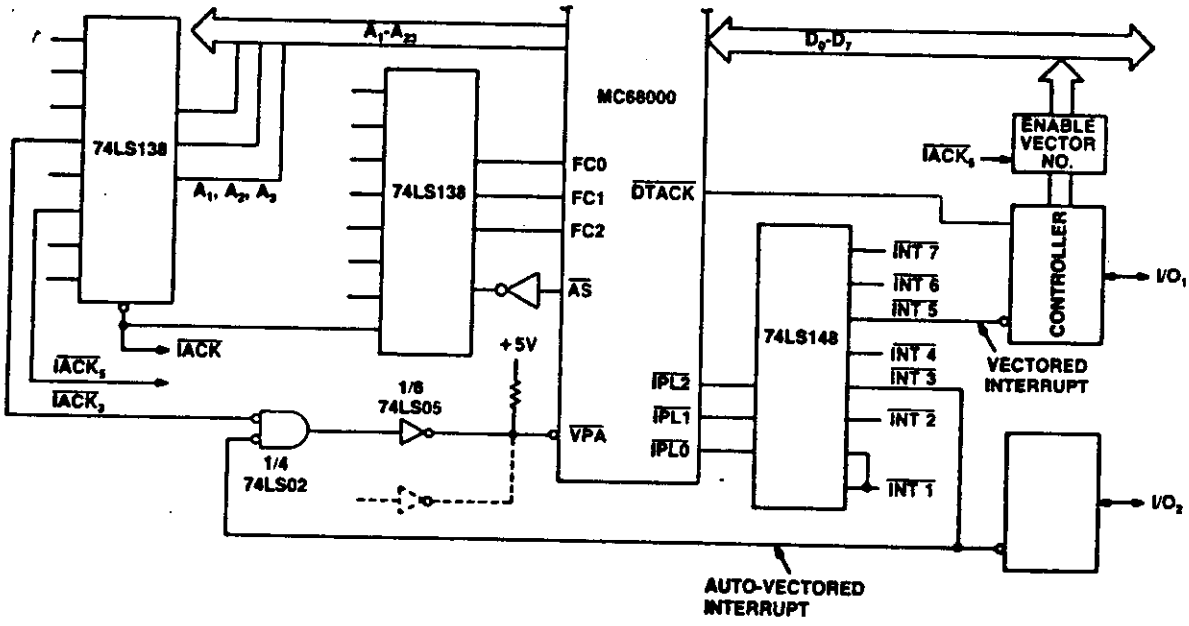
CALCULATION OF EXCEPTION VECTOR ADDRESS

VECTOR NUMBER X 4 = VECTOR ADDRESS

$0A X 4 = $28

TT624

MC68,000 — VECTORED AND AUTO-VECTORED INTERRUPT LOGIC



TT175-2

PARALLEL INTERFACE/TIMER SCN68230

Preliminary

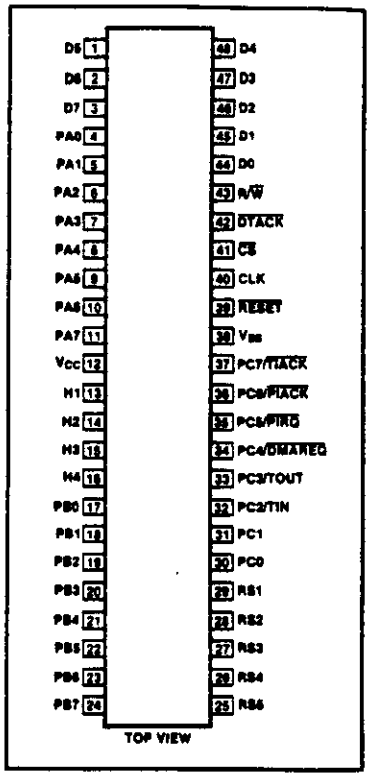
DESCRIPTION

The SCN68230 Parallel Interface/Timer (PI/T) provides versatile double buffered parallel interfaces and an operating system oriented timer to S68000 systems. The parallel interfaces operate in unidirectional or bidirectional modes, either 8 or 16 bits wide. In the unidirectional modes, an associated data direction register determines whether the port pins are inputs or outputs. In the bidirectional modes, the data direction registers are ignored and the direction is determined dynamically by the state of four handshake pins. These programmable handshake pins provide an interface flexible enough for connection to a wide variety of low, medium, or high speed peripherals or other computer systems. The PI/T ports allow use of vectored or autovectored interrupts, and also provide a DMA request pin for connection to direct memory access controllers. The PI/T timer contains a 24-bit counter and a 5-bit prescaler. The timer can be clocked by the system clock (PI/T CLK pin) or by an external clock (TIN pin), and a 5-bit prescaler can be used. It can generate periodic interrupts, a square wave or a single interrupt after a programmed time period. Also it can be used for elapsed time measurement or as a device watchdog. Table 1 is a summary of the input and output signals and Figure 1 shows the functional pin assignments. Figure 2 is a PI/T system block diagram.

FEATURES

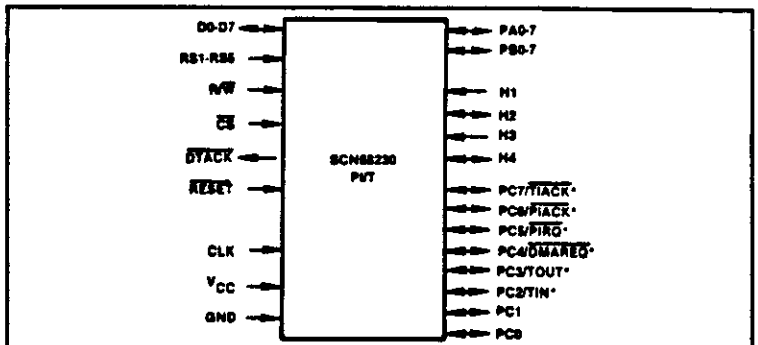
- **S68000 bus compatible**
- **Port modes include:**
  Bit I/O
  Unidirectional 8-bit and 16-bit
  Bidirectional 8-bit and 16-bit
- **Selectable handshaking options**
- **24-Bit programmable timer**
- **Software programmable timer modes**
- **Contains interrupt vector generation logic**
- **Separate port and timer interrupt service requests**
- **Registers are read/write and directly addressable**
- **Registers are addressed for MOVEP (move peripheral) and DMAC compatibility**

PIN CONFIGURATION[1]



ORDERING CODE

Packages	V_{CC} = 5V ± 5%, T_A = 0° to 70°C	
	8 MHz	10 MHz
Ceramic DIP	SCN68230C8I48	SCN68230CAI48
Plastic DIP	SCN68230C8N48	SCN68230CAN48

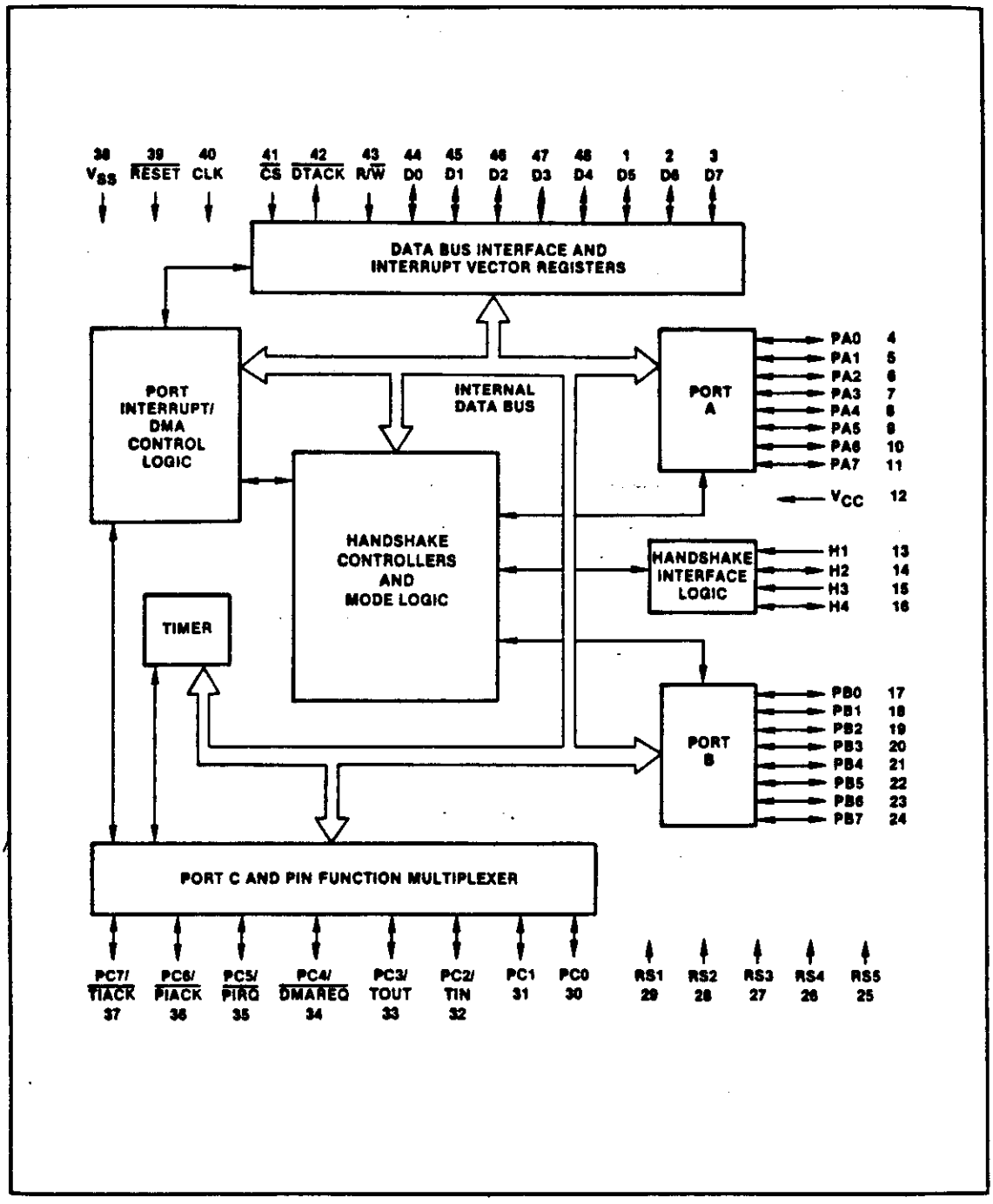


*Individually Programmable Dual-Function Pin.

Figure 1. Functional Pin Assignment

[1] In this data sheet, barring signal names (overscore) to indicate low is done only for the pin configuration diagram, signal description headings, tables and figures.

Preliminary



PARALLEL INTERFACE/TIMER SCN68230

Preliminary

Table 1 SIGNAL SUMMARY

Signal Name	Mnemonic	Input/Output	Active State	Three State
Bidirectional Data Bus	D0-D7	input/output	high	yes
Register Selects	RS1-RS5	input	high	—
Read/Write Input	R/W	input	read-high write-low	—
Chip Select	$\overline{CS}$	input	low	—
Data Transfer Acknowledge	$\overline{DTACK}$	output	low	yes
Reset	$\overline{RESET}$	input	low	—
Clock Input	CLK	input	high	—
Port A and Port B	PA0-PA7, PB0-PB7	input/output	high	yes
Handshake	H1, H3	input	programmable	—
Handshake	H2, H4	input/output	programmable	yes
Port C	PC0-PC7	input/output	high	yes
Ground	V_{SS}	input	—	—
Power Input	V_{CC}	input	—	—

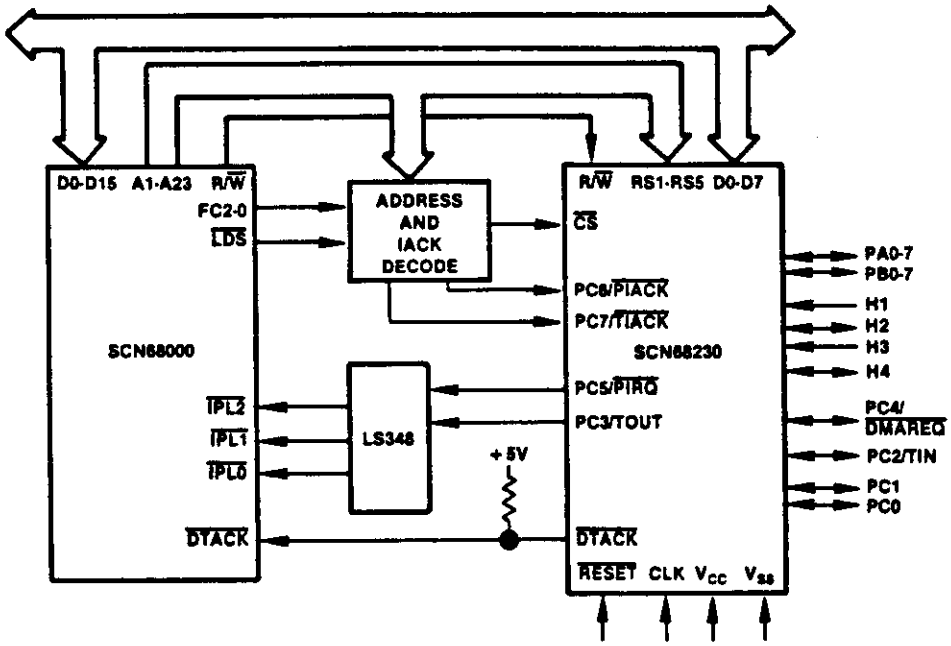


Figure 2. PI/T System Block Diagram

PARALLEL INTERFACE/TIMER SCN68230

Preliminary

GENERAL DESCRIPTION

The PI/T consists of two logically independent sections; the ports and the timer. The port section consists of port A (PA0-7), port B (PB0-7), four handshake pins (H1, H2, H3, and H4), two general I/O pins, and six dual-function pins. The dual-function pins can individually operate as a third port (port C) or an alternate function related to either ports A and B, or the timer. The four programmable handshake pins, depending on the mode, can control data transfer to and from the ports, or can be used as interrupt generating inputs, or I/O pins.

The timer consists of a 24-bit counter, optionally clocked by a 5-bit prescaler. Three pins provide complete timer I/O: PC2/TIN, PC3/TOUT, and PC7/TIACK. In specific applications, only the pins needed for the given configuration perform the timer function, while the others remain port C I/O.

The system bus interface provides for asynchronous transfer of data from the PI/T to a bus master over the data bus (D0-D7). Data transfer acknowledge (DTACK), register selects (RS1-RS5), chip select, the read/write line (R/W), and port interrupt acknowledge (PIACK) or timer interrupt acknowledge (TIACK) control data transfer between the PI/T and the SC68000.

PIN DESCRIPTIONS

D0-D7
Bidirectional data bus. The data bus pins D0-D7 form an 8-bit bidirectional data bus to/from the SCN68000 or other bus master. These pins are active high.

RS1-RS5
Register selects. RS1-RS5 are active high, high-impedance inputs that determine which of the 25 internal PI/T registers is being addressed.

R/$\overline{W}$
Read/write input. R/W is the read/write signal from the SCN68000 or bus master, indicating whether the current bus cycle is a read (high) or write (low) cycle.

$\overline{CS}$
Chip select input. The CS input selects the PI/T registers for the current bus cycle. Address strobe and the data strobe (upper or lower) of the bus master, along with the appropriate address bits, must be included in the chip select equation. A low level corresponds to an asserted chip select.

$\overline{DTACK}$
Data transfer acknowledge output. DTACK is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, DTACK is asserted by the SCN68230 after data has been provided on the data bus; during write cycles it is asserted after data has been accepted at the data bus. Data transfer acknowledge is compatible with the SCN68000 and with other bus masters such as the SCB68430 DMA controller. A holding resistor is required to maintain DTACK high between bus cycles.

$\overline{RESET}$
Reset input. RESET is used to initialize all PI/T functions. All control and data direction registers are cleared and most internal operations are disabled by the assertion of RESET (low).

CLK
Clock input. The clock pin is a TTL-compatible input with the same specifications as the SCN68000. The PI/T contains dynamic logic throughout, and hence this clock must not be gated off at any time. It is not necessary that this clock maintain any particular phase relationship with the SCN68000 clock. It can be connected to an independent frequency source (faster or slower) as long as all bus specifications are met.

PA0-PA7 and PB0-PB7
Port A and port B. Ports A and B are 8-bit ports that can be concatenated to form a 16-bit port in certain modes. The ports can be controlled in conjunction with the handshake pins H1-H4. For stabilization during system power-up, ports A and B have internal pullup resistors to V_{CC}. All port pins are active high.

H1-H4
Handshake pins (I/O depending on the mode and submode). Handshake pins H1-H4 are multi-purpose pins that (depending on the operational mode) can provide an interlocked handshake, a pulsed handshake, an interrupt input (independent of data transfers), or simple I/O pins. For stabilization during system power-up, H2 and H4 have internal pullup resistors to V_{CC}. Their sense (active high or low) can be programmed in the port general control register bits 3-0. Independent of the mode, the instantaneous level of the handshake pins can be read from the port status register.

Port C
(PC0-PC7/alternate function). This port can be used as eight general purpose I/O pins (PC0-PC7) or any combination of six special function pins and two general purpose I/O pins (PC0-PC1). (Each dual function pin can be standard I/O or a special function independent of the other port C pins.) When used as a port C pin, these pins are active high. They can be individually programmed as inputs or outputs by the Port C data direction register.

The alternate functions (TIN, TOUT, and TIACK) are timer I/O pins. TIN can be used as a rising-edge triggered external clock input or an external run/halt control pin (the timer is in the run state if run/halt is high and in the halt state if run/halt is low). TOUT can provide an active low timer interrupt request output or a general-purpose square-wave output, initially high. TIACK is an active low input used for timer interrupt acknowledge.

Port A and B functions have an independent pair of active low interrupt request (PIRQ) and interrupt acknowledge (PIACK) pins.

The DMAREQ (direct memory access request) pin provides an active low direct memory access controller (DMAC) request pulse of three clock cycles.

REGISTER MODEL

A register model that includes the corresponding register selects is shown in Table 2.

PORT FUNCTIONAL DESCRIPTION

Port Control Structure
The primary focus of most applications will be on ports A and B, the handshake pins, the port interrupt pins, and the DMA request pin. The ports are controlled by the port general control register which contains a 2-bit field that specifies a set of four operation modes. These govern the overall operation of the ports and determine their interrelationships. Some modes require additional information from each port's control register to further define its operation. In each port control register, there is a 2-bit submode field that serves this purpose. Each port mode/submode combination specifies a set of programmable characteristics that fully define the behavior of that port and two of the handshake pins. This structure is summarized in Table 3 and Figure 3.

Preliminary

Table 3 PORT MODE CONTROL SUMMARY

Mode 0 (Unidirectional 8-Bit Mode)
- Port A
  - Submode 00 — Double-Buffered Input
    - H1 — Latches input data
    - H2 — Status/interrupt generating input, general-purpose output, or operation with H1 in the interlocked or pulsed input handshake protocols
  - Submode 01 — Double-Buffered Output
    - H1 — Indicates data received by peripheral
    - H2 — Status/interrupt generating input, general-purpose output, or operation with H1 in the interlocked or pulsed output handshake protocols
  - Submode 1X — Bit I/O
    - H1 — Status/interrupt generating input
    - H2 — Status/interrupt generating input or general-purpose output
- Port B, H3 and H4 — Identical to Port A, H1 and H2

Mode 1 (Unidirectional 16-Bit Mode)
- Port A — Double-Buffered Data (Most significant)
  - Submode XX (not used)
    - H1 — Status/interrupt generating input
    - H2 — Status/interrupt generating input or general-purpose output
- Port B — Double-Buffered Data (Least significant)
  - Submode X0 — Unidirectional 16-Bit Input
    - H3 — Latches input data
    - H4 — Status/interrupt generating input, general-purpose output, or operation with H3 in the interlocked or pulsed input handshake protocols
  - Submode X1 — Unidirectional 16-Bit Output
    - H3 — Indicates data received by peripheral
    - H4 — Status/interrupt generating input, general-purpose output, or operation with H3 in the interlocked or pulsed output handshake protocols

Mode 2 (Bidirectional 8-Bit Mode)
- Port A — Bit I/O (with no handshaking pins)
  - Submode XX (not used)
- Port B — Bidirectional 8-Bit Data (Double-Buffered)
  - Submode XX (not used)
    - H1 — Indicates output data received by peripheral
    - H2 — Operation with H1 in the interlocked or pulsed output handshake protocols
    - H3 — Latches input data
    - H4 — Operation with H3 in the interlocked or pulsed input handshake protocols

Mode 3 (Bidirectional 16-Bit Mode)
- Port A — Double-Buffered Data (Most significant)
  - Submode XX (not used)
- Port B — Double-Buffered Data (Least significant)
  - Submode XX (not used)
- H1 — Indicates output data received by peripheral
- H2 — Operation with H1 in the interlocked or pulsed output handshake protocols
- H3 — Latches input data
- H4 — Operation with H3 in the interlocked or pulsed input handshake protocols

Port General Information and Conventions
The following paragraphs introduce concepts that are generally applicable to the PI/T ports independent of the chosen mode and submode. For this reason, no particular port or handshake pins are mentioned; the notation H1 (H3) indicates that, depending on the chosen mode and submode, the statement given may be true for either the H1 or H3 handshake pin.

Unidirectional vs Bidirectional—Figure 3 shows the configuration of ports A and B and each of the handshake pins in each port mode and submode. In modes 0 and 1, a data direction register is associated with each of the ports. These registers contain one bit for each port pin to determine whether that pin is an input or an output. Modes 0 and 1 are, thus, called unidirectional modes because each pin assumes a constant direction, changeable only by a reset condition or a programming change. These modes allow double buffered data transfers in one direction. This direction, determined by the mode and submode definition, is known as the primary direction. Data transfers in the primary direction are controlled by the handshake pins. Data transfers not in the primary direction are generally unrelated, and single or unbuffered data paths exist.

In modes 2 and 3 there is no concept of primary direction as in modes 0 and 1. Except for port A in mode 2 (bit I/0), the data direction registers have no effect. These modes are bidirectional, in that the direction of each transfer (always 8 or 16 bits, double buffered) is determined dynamically by the state of the handshake pins. Thus, for example, data may be transferred out of the ports, followed very shortly by a transfer into the same port pins. Transfers to and from the ports are independent and may occur in any sequence. Since the instantaneous direction is always determined by the external system, a small amount of arbitration logic may be required.

Control of Double Buffered Data Paths—Generally speaking, the PI/T is a double buffered device. In the primary direction, double buffering allows orderly transfers by using the handshake pins in any of several programmable protocols. (When bit I/0 is used, double buffering is not available and the handshake pins are used as outputs or status/interrupt inputs.)

Preliminary

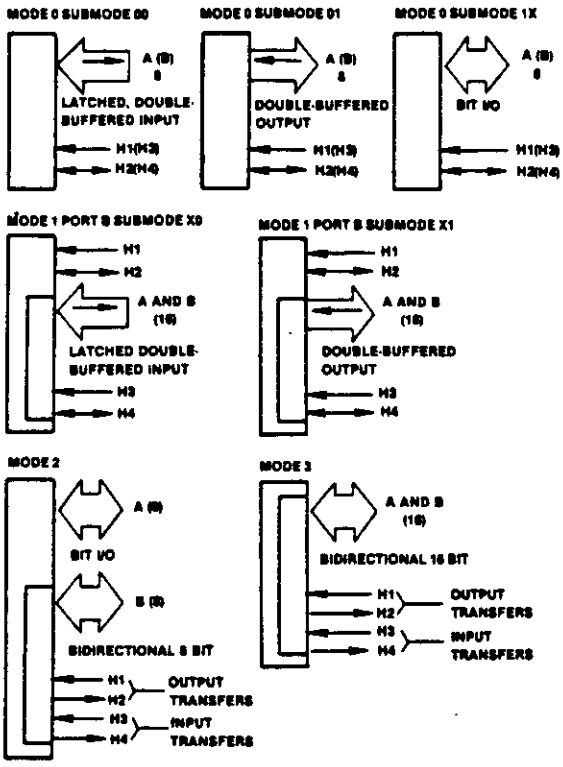


Figure 3. Port Mode Layout

Use of double buffering is most beneficial in situations where a peripheral device and the computer system are capable of transferring data at roughly the same speed. Double buffering allows the fetch operation of the data transmitter to be overlapped with the store operation of the data receiver. Thus, throughput measured in bytes or words per second can be greatly enhanced. If there is a large mismatch in transfer capability between the computer and the peripheral, little or no benefit is obtained. In these cases there is no penalty in using double buffering.

Double Buffered Input Transfers—In all modes, the PI/T supports double buffered input transfers. Data that meets the port setup and hold times is latched on the asserted edge of H1(H3). H1(H3) is edge sensitive, and may assume any duty cycle as long as both high and low minimum times are observed. The PI/T contains a port status register whose H1S(H3S) status bit is set anytime any input data is present in the double buffered latches that has not been read by the bus master. The action of H2(H4) is programmable; it may indicate whether there is room for more data in the PI/T latches or it may serve other purposes. The following options are available, depending on the mode.

1. H2(H4) may be an edge sensitive input that is independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S(H4S) status bit is set. It is cleared by the direct method (refer to Direct Method of Resetting Status), the RESET pin being asserted, or when the H12 enable (H34 enable) bit of the port general control register is 0.
2. H2(H4) may be a general purpose output pin that is always negated. The H2S(H4S) status bit is always 0.
3. H2(H4) may be a general purpose output pin that is always asserted. The H2S(H4S) status bit is always 0.
4. H2(H4) may be an output pin in the interlocked input handshake protocol. It is asserted when the port input latches are ready to accept new data. It is negated asynchronously following the asserted edge of the H1(H3) input. As soon as the input latches become ready, H2(H4) is again asserted. When the input double buffered latches are full, H2(H4) remains negated until data is removed. Thus, anytime the H2(H4) output is asserted, new input data may be entered by asserting H1(H3). At other times, transitions on H1(H3) are ignored. The H2S(H4S) status bit is always 0. When H12 enable (H34 enable) is 0, H2(H4) is held negated.
5. H2(H4) may be an output pin in the pulsed input handshake protocol. It is asserted exactly as in the interlocked input protocol, but never remains asserted longer than 4 clock cycles. Typically, a four clock cycle pulse is generated. But in the case where a subsequent H1(H3) asserted edge occurs before termination of the pulse, H2(H4) is negated asynchronously. Thus, anytime after the leading edge of the H2(H4) pulse, new data can be entered in the PI/T double buffered input latches. The H2S(H4S) status bit is always 0. When H12 enable (H34 enable) is 0, H2(H4) is held negated.

A sample timing diagram is shown in Figure 4. The H2(H4) interlocked and pulsed input handshake protocols are shown. The DMAREQ pin is also shown assuming it is enabled. All handshake pin sense bits are assumed to be 0 (refer to Port General Control Register); thus, the pins are in the low state when asserted. Due to the great similarity between modes, this timing diagram is applicable to all double buffered input transfers.

Double Buffered Output Transfers—The PI/T supports double buffered output transfers in all modes. Data, written by the bus master to the PI/T, is stored in the port's output latch. The peripheral accepts the data by asserting H1(H3), which causes the next data to be moved to the port's output latch as soon as it is available. The function of H2(H4) is programmable; it may indicate whether new

Preliminary

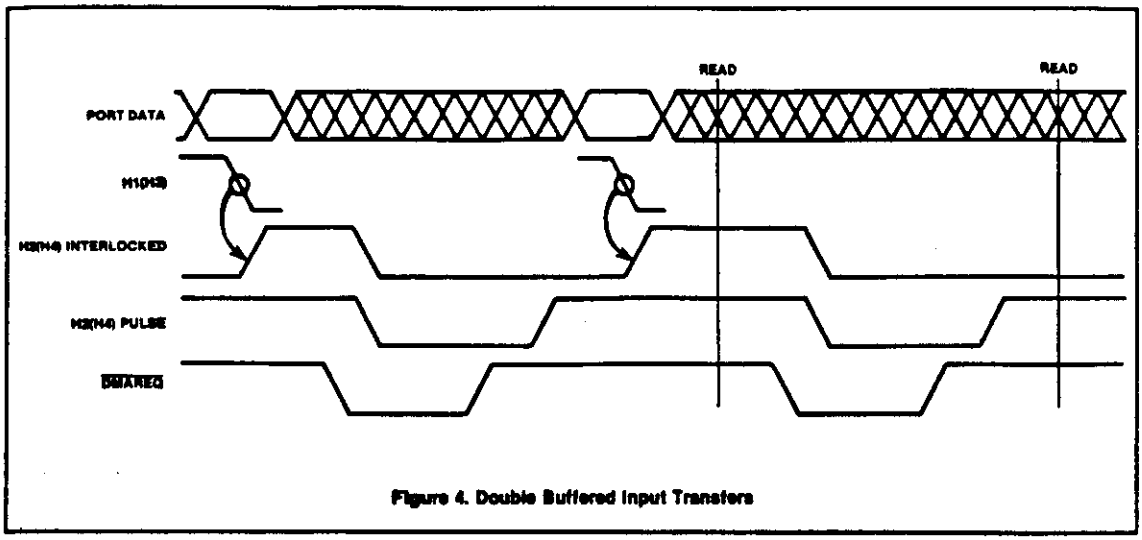


Figure 4. Double Buffered Input Transfers

data has been moved to the output latch or it may serve other purposes. The H1S(H3S) status bit may be programmed for two interpretations. Normally the status bit is a 1 when there is at least one latch in the double buffered data path that can accept new data. After writing one byte/word of data to the ports, an interrupt service routine could check this bit to determine if it could store another byte/word; thus, filling both latches. When the bus master is finished, it is often useful to be able to check whether all of the data has been transferred to the peripheral. The H1S(H3S) status control bit of the port A and B control registers provide this flexibility. The programmable options of the H2(H4) pin are given below, depending on the mode.

1. H2(H4) may be an edge sensitive input pin independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S (H4S) status bit is set. It is reset by the direct method (refer to Direct Method of Resetting Status), the RESET pin being asserted, or when the H12 enable (H34 enable) bit of the port general control register is 0.

2. H2(H4) may be a general purpose output pin that is always negated. The H2S(H4S) status bit is always 0.

3. H2(H4) may be a general purpose output pin that is always asserted. The H2S(H4S) status bit is always 0.

4. H2(H4) may be an output pin in the interlocked output handshake protocol. H2(H4) is asserted two clock cycles after data is transferred to the double buffered output latches. The data remains stable and H2(H4) remains asserted until the next asserted edge of the H1(H3) input. At that time, H2(H4) is asynchronously negated. As soon as the next data is available, it is transferred to the output latches. When H2(H4) is negated, asserted transitions on H1(H3) have no effect on the data paths. As is explained later, however, in modes 2 and 3 they do control the three-state output buffers of the bidirectional port(s). The H2S(H4S) status bit is always 0. When H12 enable (H34 enable) is 0, H2(H4) is held negated.

5. H2(H4) may be an output pin in the pulsed output handshake protocol. It is asserted exactly as in the interlocked output protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock pulse is generated. But in the case where a subsequent H1(H3) asserted edge occurs before termination of the pulse, H2(H4) is negated asynchronously shortening the pulse. The H2S(H4S) status bit is always 0. When H12 enable (H34 enable) is 0, H2(H4) is held negated.

A sample timing diagram is shown in Figure 5. The H2(H4) interlocked and pulsed output handshake protocols are shown. The DMAREQ pin is also shown assuming it is enabled. All handshake pin sense bits are assumed to be 0; thus, the pins are in the low state when asserted. Due to the great similarity between modes, this timing diagram is applicable to all double buffered output transfers.

Requesting Bus Master Service—The PI/T has several means of indicating a need for service by a bus master. First, the processor may poll the port status register. It contains a status bit for each handshake pin, plus a level bit that always reflects the instantaneous state of that handshake pin. A status bit is 1 when the PI/T needs servicing, i.e., generally when the bus master needs to read or write data to the ports, or when a handshake pin used as a simple status input has been asserted. The interpretation of these bits is dependent on the chosen mode and submode.

Second, the PI/T may be placed in the processor's interrupt structure. As mentioned previously, the PI/T contains port A and B control registers that configure the handshake pins. Other bits in these registers enable an interrupt associated with each handshake pin. This interrupt is made available through the PC5/PIRQ pin, if the PIRQ function is selected. Three additional conditions are required for PIRQ to be asserted: (1) the handshake pin status bit is set, (2) the corresponding interrupt (service request) enable bit is set, and (3) DMA requests are not associated with that data transfer (H1 and H3 only).

Preliminary

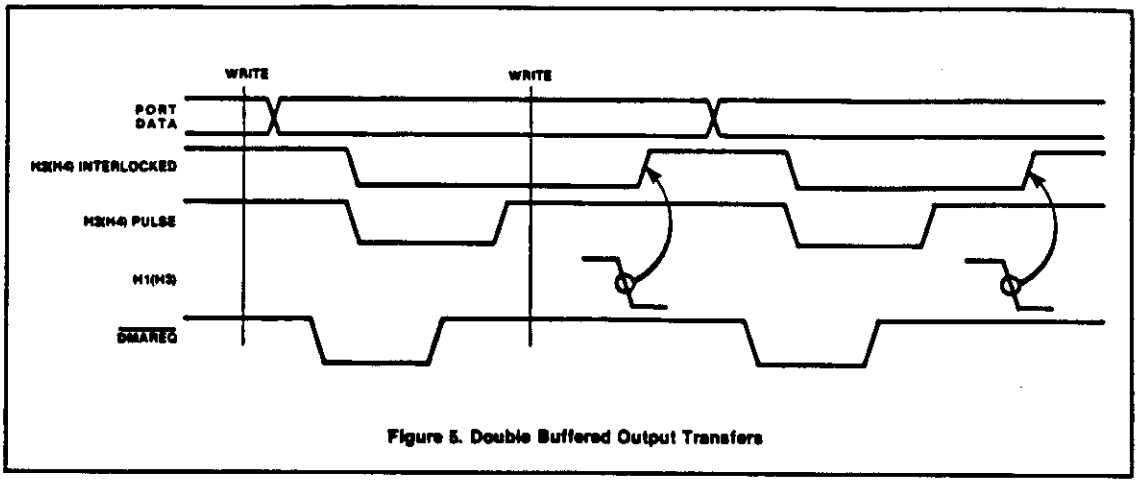


Figure 5. Double Buffered Output Transfers

The conditions from each of the four handshake pins and corresponding status bits are ORed to determine PIRQ.

The third method of requesting service is via the PC4/DMAREQ pin. This pin can be associated with double buffered transfers in each mode. If it is used as a DMA controller request, it can initiate requests to keep the PI/T's input/output double buffering empty/full as much as possible. It will not overrun the DMA controller.

Vectored, Prioritized Port Interrupts—Use of SCN68000 compatible vectored interrupts with the PI/T requires the PIRQ and PIACK pins. When PIACK is asserted, the PI/T places an 8-bit vector on the data pins D0-D7. Under normal conditions, this vector corresponds to highest priority, enabled, active port interrupt source with which the DMAREQ pin is not currently associated. The most significant six bits are provided by the port interrupt vector register (PIVR), with the lower two bits supplied by prioritization logic according to conditions present when PIACK is asserted. It is important to note that the only effect on the PI/T caused by interrupt acknowledge cycles is that the vector is placed on the data bus. Specifically, no registers, data, status, or other internal states of the PI/T are affected by the cycle.

Several conditions may be present when the PIACK input is asserted. These conditions affect the PI/T's response and the termination of the bus cycle. If the PI/T has no interrupt function selected, or is not asserting PIRQ, the PI/T will make no response to PIACK (DTACK will not be asserted). If the PI/T is asserting PIRQ when PIACK is received, the PI/T will output the contents of the PIVR and the prioritization bits. If the PIVR has not been initialized, $0F will be read from this register. These conditions are summarized in Table 4.

The vector table entries for the PI/T appear as a contiguous block of four vector numbers whose common upper six bits are programmed in the PIVR. The following list pairs each interrupt source with the 2-bit value provided by the prioritization logic, when interrupt acknowledge is asserted.

H1 source—00
H2 source—01
H3 source—10
H4 source—11

Autovectored Port Interrupts—Autovectored interrupts use only the PIRQ pin. The operation of the PI/T with vectored and autovectored interrupts is identical except that no vectors are supplied and the PC6/PIACK pin can be used as a port C pin.

Direct Method of Resetting Status—In certain modes one or more handshake pins can be used as edge sensitive inputs for the sole purpose of setting bits in the port status register. These bits consist of simple flip flops. They are set (to 1) by the occurrence of the asserted edge of the handshake pin input. Resetting a handshake status bit can be done by writing an 8-bit mask to the port status register. This is called the direct method of resetting. To reset a status bit that is resettable by the direct method, the mask must contain a 1 in the bit position of the port status register corresponding to the desired bit. Other positions must contain 0's. For status bits that are not resettable by the direct method in the chosen mode, the data written to the port status register has no effect. For status bits that are resettable by the direct method in the chosen mode, a 0 in the mask has no effect.

Handshake Pin Sense Control—The PI/T contains exclusive OR gates to control the

Table 4 RESPONSE TO PORT INTERRUPT ACKNOWLEDGE

Conditions	PIRQ negated OR interrupt request function not selected	PIRQ asserted
PIVR has not been initialized since RESET	No response from PI/T. No DTACK	PI/T provides $0F, the Uninitialized Vector *
PIVR has been initialized since RESET	No response from PI/T. No DTACK	PI/T provides PIVR contents with prioritization bits.

*The uninitialized vector is the value returned from an interrupt vector register before it has been initialized.

Preliminary

sense of each of the handshake pins, whether used as inputs or outputs. Four bits in the port general control register can be programmed to determine whether the pins are asserted in the low or high voltage state. As with other control registers, these bits are reset to 0 when the RESET pin is asserted, defaulting the asserted level to be low.

Enabling Ports A and B—Certain functions involved with double buffered data transfers, the handshake pins, and the status bits, can be disabled by the external system or by the programmer during initialization. The port general control register contains two bits, H12 enable and H34 enable, which control these functions. These bits are cleared to the 0 state when the RESET pin is asserted, and the functions are disabled. The functions are the following:

1. Independent of other actions by the bus master or peripheral (via the handshake pins), the PI/T's disabled handshake controller is held to the 'empty' state, i.e., no data is present in the double buffered data path.

2. When any handshake pin is used to set a simple status flip flop, unrelated to double buffered transfers, these flip flops are held reset to 0 (see Table 3).

3. When H2(H4) is used in an interlocked or pulsed handshake with H1(H3), H2(H4) is held negated, regardless of the chosen mode, submode, and primary direction. Thus, for double buffered input transfers, the programmer can signal a peripheral when the PI/T is ready to begin transfers by setting the associated handshake enable bit to 1.

The Port A and B Alternate Registers—In addition to the port A and B data registers, the PI/T contains port A and B alternate registers. These registers are read only, and simply provide the instantaneous level of each port pin. They have no effect on the operation of the handshake pins, double buffered transfers, status bits, or any other aspect of the PI/T, and they are mode/submode independent.

PORT MODES

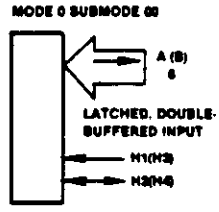
Mode 0—Unidirectional 8-Bit Mode
In mode 0, ports A and B operate independently. Each can be configured in any of its three possible submodes:

Submode 00—Double buffered input
Submode 01—Double buffered output
Submode 1X—Bit I/O

Handshake pins H1 and H2 are associated with port A and configured by programming the port A control register. (The H12 enable bit of the port general control register enables port A transfers.) Handshake pins H3 and H4 are associated with port B and configured by programming the port B control register. (The H34 enable bit of the port general control register enables port B transfers.) The port A and B data direction registers operate in all three submodes. Along with the submode, they affect the data read and written at the associated data register according to Table 5. They also enable the output buffer associated with each port pin. The DMAREQ pin may be associated with either (not both) port A or port B, but does not function if the bit I/O submode is programmed for the chosen port.

Port A or B Submode 00 (8-Bit Double Buffered Input)—In mode 0, double buffered input transfers of up to 8-bits are available by programming submode 00 in the desired port's control register. The operation of H2 and H4 can be selected by programming the port A and port B control registers, respectively. All five double buffered input handshake options, previously mentioned in the Port General Information and Conventions section, are available.

For pins used as outputs, the data path consists of a single latch driving the output buffer. Data written to the port's data register does not affect the operation of any handshake pin, status bit, or any other aspect of the PI/T. Output pins can be used independently of the input transfer. However, read bus cycles to the data register do remove data from the port. Therefore, care should be taken to avoid processor instructions that perform unwanted read cycles. Refer to Figure 4 for a sample timing diagram.



Port A or B Submode 01 (8-bit Double Buffered Output)—In mode 0, double buffered output transfers of up to 8 bits are available by programming submode 01 in the desired port's control register. The operation of H2 and H4 can be selected by programming the port A and port B control registers, respectively. All five double buffered output handshake options, previously mentioned in the Port General Information and Conventions section, are available.

For pins used as inputs, data written to the associated data register is double buffered and passed to the initial or final output latch, as usual, but the output buffer is disabled. Refer to Figure 5 for a sample timing diagram.

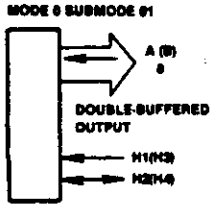


Table 5 MODE 0 PORT DATA PATHS

Mode	Read Port A/B Data Register		Write Port A/B Data Register	
	DDR = 0	DDR = 1	DDR = X	
0 Submode 00	FIL, D.B.	FOL Note 3	FOL, S.B.	Note 1
0 Submode 01	Pin	FOL Note 3	IOL/FOL, D.B.	Note 2
0 Submode 1X	Pin	FOL Note 3	FOL, S.B.	Note 1

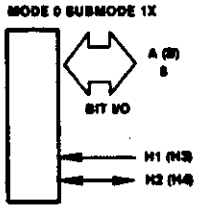
Abbreviations:
IOL – Initial Output Latch
FOL – Final Output Latch
FIL – Final Input Latch
S.B. – Single Buffered
D.B. – Double Buffered
DDR – Data Direction Register

Note 1: Data is latched in the output data registers (final output latch) and will be single buffered at the pin if the DDR is 1. The output buffers will be turned off if the DDR is 0.
Note 2: Data is latched in the double-buffered output data registers. The data in the final output latch will appear on the port pin if the DDR is a 1.
Note 3: The output drivers that connect the final output latch to the pins are turned on.

Preliminary

Port A or B Submode 1X (Bit I/O)—In mode 0, simple bit I/O is available by programming submode 1X in the desired port's control register. This submode is intended for applications in which several independent devices must be controlled or monitored. Data written to the associated data register is single buffered. If the data direction register bit for that pin is a 1 (output), the output buffer is enabled. If it is 0 (input), data written is still latched, but is not available at the pin. Data read from the data register is the instantaneous value of the pin or what was written to the data register, depending on the contents of the data direction register. H1(H3) is an edge sensitive status input pin only and it controls no data related function. The H1S(H3S) status bit is set following the asserted edge of the input waveform. It is reset by the direct method, the RESET pin being asserted, or when the H12 enable (H34 enable) bit is 0.

H2(H4) can be programmed as a simple status input (identical to H1(H3)), or as an asserted or negated output. The interlocked or pulsed handshake configurations are not available.



Mode 1—Unidirectional 16-Bit Mode
In mode 1, ports A and B are concatenated to form a single 16-bit port. The port B submode field controls the configuration of both parts. The possible submodes are:

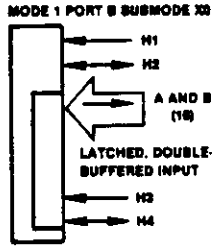
Port B submode X0—double buffered input
Port B submode X1—double buffered output

Handshake pins H3 and H4, configured by programming the port B control register, are associated with the 16-bit double buffered transfer. These 16-bit transfers are enabled by the H34 enable bit of the port general control register. Handshake pins H1 and H2 can be used as simple status inputs not related to the 16-bit data transfer or H2 can be an output. Enabling of the H1 and H2 handshake pins is done by the H12 enable bit of the port general control register. The port A and B data direction registers operate in each submode. Along with the submode, they affect the data read and written at the data register according to Table 6. They also enable the output buffer associated with each port pin. The DMAREQ pin can be associated only with H3.

Mode 1 can provide convenient, high speed 16-bit transfers. The port A and B data registers are addressed for compatibility with the SCN68000 move peripheral (MOVEP) instruction and with the S68000 DMA controllers. To take advantage of this, port A should contain the most significant byte of data and always be read or written by the bus master first. The interlocked and pulsed handshake protocols are keyed to accesses to the port B data register in mode 1. If it is accessed last, the 16-bit double buffered transfers proceed smoothly.

Port B Submode X0 (16-Bit Double Buffered Input)—In mode 1 port B submode X0, double buffered input transfers of up to 16-bits can be obtained. The level of all 16 pins is asynchronously latched with the asserted edge of H3. The processor can check the H3S status bit to determine if new data is present. The DMAREQ pin can be used to signal a DMA controller to empty the input buffers. Regardless of the bus master, port A data should be read first. (Actually, port A data need not be read at all.) Port B data should be read last. The operation of the internal handshake controller, the H3S bit, and DMAREQ are keyed to the reading of the port B data register. (The S68000 DMA controllers can be programmed to perform the exact transfers needed for compatibility with the PI/T.) H4 can be programmed for all five of the handshake options mentioned in the Port General Information and Conventions section.

For pins used as outputs, the data path consists of a single latch driving the output buffer. Data written to the port's data register does not affect the operation of any handshake pin, status bit, or any other aspect of the PI/T. Thus, output pins can be used independently of the input transfer. However, read bus cycles to the port B data register do remove data, so care should be taken to avoid unwanted read cycles.



Port B Submode X1 (16-Bit Double Buffered Output)—Refer to Figure 4 for a sample timing diagram. In mode 1 port B submode X1, double buffered output transfers of up to 16 bits can be obtained. Data is written by the bus master (processor or DMA controller) in two bytes. The first byte (most significant) is written to the port A data register. It is stored in a temporary latch until the next byte is written to the port B data register. Then all 16 bits are transferred to the final output latches

Table 6 MODE 1 PORT DATA PATHS

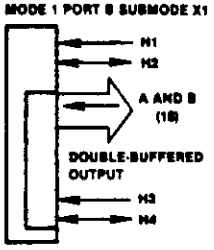
Mode	Read Port A/B Register		Write Port A/B Register	
	DDR = 0	DDR = 1	DDR = 0	DDR = 1
1, Port B Submode X0	FIL, D.B.	FOL Note 3	FOL, S.B. Note 2	FOL, S.B. Note 2
1, Port B Submode X1	Pin	FOL Note 3	IOL/FOL, D.B., Note 1	IOL/FOL, D.B., Note 1

Note 1: Data written to Port A goes to a temporary latch. When the Port B data register is later written, Port A data is transferred to IOL/FOL.
Note 2: Data is latched in the output data registers (final output latch) and will be single buffered at the pin if the DDR is 1. The output buffers will be turned off if the DDR is 0.
Note 3: The output drivers that connect the final output latch to the pins are turned on.

Abbreviations:
IOL – Initial Output Latch
FOL – Final Output Latch
FIL – Final Input Latch
S.B. – Single Buffered
D.B. – Double Buffered
DDR – Data Direction Register

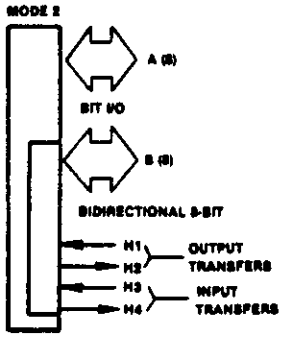
of ports A and B. Both options for interpretation of the H3S status bit, mentioned in Port General Information and Comments section, are available and apply to the 16-bit port as a whole. The DMAREQ pin can be used to signal a DMA controller to transfer another word to the port output latches. (The S68000 DMA controllers can be programmed to perform the exact transfers needed for compatibility with the PI/T.) H4 can be programmed for all five of the handshake options mentioned in the Port General Information and Conventions section.

For pins used as inputs, data written to either data register is double buffered and passed to the initial or final output latch, as usual, but the output buffer is disabled. Refer to Figure 5 for a sample timing diagram.



Mode 2—Bidirectional 8-Bit Mode

In mode 2, port A is used for simple bit I/O with no associated handshake pins. Port B is used for bidirectional 8-bit double buffered transfers. H1 and H2, enabled by the H12 enable bit in the port general control register, control output transfers, while H3 and H4, enabled by the port general control register H34 enable bit, control input transfers. The instantaneous direction of the data is determined by the H1 handshake pin. The port B data direction register is not used. The port A and port B submode fields do not affect the PI/T operation in mode 2.



Double Buffered I/O (Port B)—The only aspect of bidirectional double buffered transfers that differs from the unidirectional modes lies in controlling the port B output buffers. They are controlled by the level of H1. When H1 is negated, the port B output buffers (all eight) are enabled and the pins drive the bidirectional bus. Generally, H1 is negated in response to an asserted H2 which indicates that new output data is present in the double buffered latches. Following acceptance of the data, the peripheral asserts H1 disabling the port B output buffers. Other than controlling the output buffer, H1 is edge sensitive as in other modes. Input transfers proceed identically to the double buffered input protocol described in the Port General Information and Conventions Section. In mode 2, only the interlocked and pulsed handshake pin options are available on H2 and H4. The DMAREQ pin can be associated with either input transfers (H3) or output transfers (H1), but not both. Refer to Table 7 for a summary of the port B data register responses in mode 2.

Bit I/O (Port A)—In mode 2, port A performs simple bit I/O with no associated handshake pins. This configuration is intended for applications in which several independent devices must be controlled or monitored. Data written to the port A data register is single buffered. If the port A data direction register bit for that pin is 1 (output), the output buffer is enabled. If it is 0, data written is still latched but not available at the pin. Data read from the data register is either the instantaneous value of the pin or what was written to the data register, depending on the contents of the port A data direction register. This is summarized in table 8.

Mode 3—Bidirectional 16-Bit Double Buffered I/O

In mode 3, ports A and B are used for bidirectional 16-bit double buffered transfers. H1 and H2 control output transfers, while H3 and H4 control input transfers. (H1 and H2 are enabled by the H12 enable bit while H3 and H4 are enabled by the H34 enable bit of the port general control register.) The instantaneous direction of the data is determined by the H1 handshake pin, and thus, the data direction registers are not used. The port A and port B submode fields do not affect PI/T operation in mode 3.

The only aspect of bidirectional double buffered transfers that differs from the unidirectional modes lies in controlling the port A and B output buffers. They are controlled by the level of H1. When H1 is negated, the output buffers (all 16) are enabled and the pins drive the bidirectional bus. Generally, H1 is negated in response to an asserted H2, which indicates that new output data is present in the double buffered latches. Following acceptance of the data, the peripheral asserts H1, disabling the output buffers. Other than controlling the output buffers, H1 is edge sensitive as in other modes. Input transfers proceed identically to the double buffered input protocol described in the Port General Information and Conventions section. Port A and B data is latched with the asserted edge of H3. In

Table 7 MODE 2 PORT B DATA PATHS

Mode	Read Port B Data Register	Write Port B Data Register
2	FIL. D.B	IOL/FOL. D.B

Abbreviations:
IOL – Initial Output Latch
FOL – Final Output Latch
FIL – Final Input Latch
D.B. – Double Buffered

Table 8 MODE 2 PORT A DATA PATHS

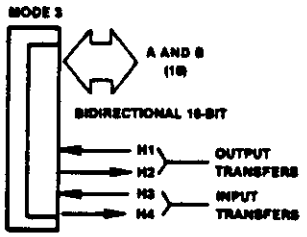
Mode	Read Port A Data Register		Write Port A Data Register	
	DDR = 0	DDR = 1	DDR = 0	DDR = 1
2	Pin	FOL	FOL	FOL. S.B

Abbreviations:
S.B. – Single Buffered
FOL – Final Output Latch
DDR – Data Direction Register

Preliminary

mode 3, only the interlocked and pulsed handshake pin options are available to H2 and H4. The DMAREQ pin can be associated with either input transfers (H3) or output transfers (H1), but not both. H2 indicates when new data is available in the port B (and implicitly port A) output latches, but unless the buffer is enabled by H1, the data is not driving the pins.

Mode 3 can provide convenient high speed 16-bit transfers. The port A and B data registers are addressed for compatibility with the SCN68000's move peripheral (MOVEP) instruction and with the S68000 DMA controllers. To take advantage of this, port A should contain the most significant data and always be read or written by the bus master first. The interlocked and pulsed handshake protocols are keyed to accesses to the port B data register in mode 3. If it is accessed last, the 16-bit double buffered transfer proceeds smoothly. Refer to Table 9 for a summary of the port A and B data paths in mode 3.



DMA REQUEST OPERATION

The direct memory access request (DMAREQ) pulse (when enabled) is associated with output or input transfers to keep the initial and final output latches full or empty, respectively. Figures 6 and 7 show all the possible paths in generating DMA requests.

DMAREQ is generated on the bus side of the SCN68230 by the synchronized[1] chip select. If the conditions of Figures 6 and 7 are met, an access of the bus (assertion of CS) will cause DMAREQ to be asserted three PI/T clocks (plus the delay time from the clock edge) after CS is synchronized. DMAREQ remains asserted for three clock cycles (plus the delay time from the clock edge) and is then negated.

[1]Synchronized means that the input signal has been seen by the PI/T on the appropriate edge of the clock (rising edge for H1(H3) and falling edge for CS). (Refer to the Bus Interface section for the exception concerning CS.) If a bus access (assertion of CS) and a port access (assertion of H1(H3)) occur at the same time, CS will be recognized without delay. H1(H3) will be recognized one clock cycle later.

Table 9 MODE 3 PORT A AND B DATA PATHS

Mode	Read Port A and B Data Register	Write Port A and B Data Register
3	FIL, D.B	IOL/FOL, D.B., Note 1

Note 1: Data written to Port A goes to a temporary latch. When the Port B data register is later written, Port A data is transferred to IOL/FOL.

Abbreviations:
IOL – Initial Output Latch
FOL – Final Output Latch
FIL – Final Input Latch
S.B. – Single Buffered
D.B. – Double Buffered

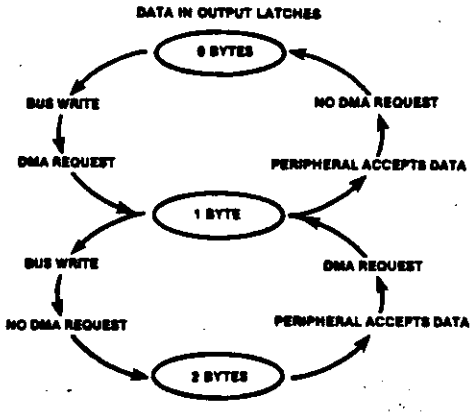


Figure 6. DMAREQ Associated with Output Transfers

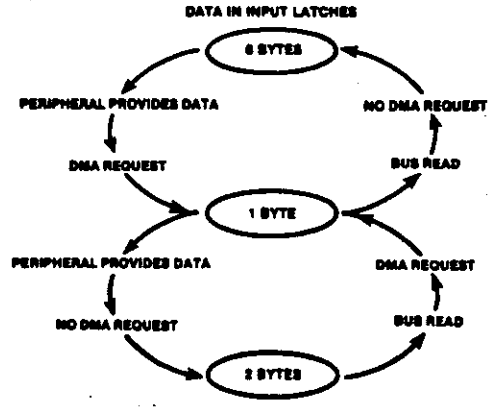


Figure 7. DMAREQ Associated with Input Transfers

Preliminary

The DMAREQ pulse associated with a peripheral or port side of the PI/T is caused by the synchronized H1(H3) input. If the conditions of figures 6 and 7 are met, a port access (assertion of the H1(H3) input) will cause DMAREQ to be asserted 2.5 PI/T clock cycles (plus the delay time from clock edge) after H1(H3) is synchronized. DMAREQ remains asserted for three clock cycles (plus the delay time from the clock edge) and is then negated.

TIMER

The SCN68230 timer can provide several facilities needed by S68000 operating systems. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. Also, it can be used for elapsed time measurement or as a device watchdog.

The PI/T timer contains a 24-bit synchronous down counter that is loaded from three 8-bit counter preload registers. The 24-bit counter can be clocked by the output of a 5-bit (divide by 32) prescaler or by an external timer input TIN. If the prescaler is used, it can be clocked by the system clock (CLK pin) or by the TIN external input. The counter signals the occurrence of an event primarily through zero detection. (A zero is when the value of the 24-bit timer is equal to zero.) This sets the zero detect status (ZDS) bit in the timer status register. It can be checked by the processor or can be used to generate a timer interrupt. The ZDS bit is reset by writing a 1 to the timer status register in that bit position.

The general operation of the timer is flexible and easily programmable. The timer is fully configured and controlled by programming the 8-bit timer control register. It controls the choice between the port C operation and the timer operation of three timer pins, whether the counter is loaded from the counter preload register or rolls over when zero detect is reached, the clock input, whether the prescaler is used, and whether the timer is enabled.

Run/Halt Definition

The overall operation of the timer is described in terms of the run or halt states. The control of the current state is determined by programming the timer control register. When in the halt state, all of the following occur:

1. The prior contents of the counter is not altered and is reliably readable via the count registers.
2. The prescaler is forced to $1F whether or not it is used.
3. The ZDS status bit is forced to 0, regardless of the possible zero contents of the 24-bit counter.

The run state is characterized by:

1. The counter is clocked by the source programmed in the timer control register.
2. The counter is not reliably readable.
3. The prescaler is allowed to decrement if programmed for use.
4. The ZDS status bit is set when the 24-bit counter transitions from $000001 to $000000.

Timer Rules

This following set of rules allow easy application of the timer.

1. Refer to the run/halt definition above.
2. When the RESET pin is asserted, all bits of the timer control register go to 0, configuring the dual function pins as port C inputs.
3. The contents of the counter preload registers and counter are not affected by the RESET pin.
4. The count registers provide a direct read data path from each portion of the 24-bit counter, but data written to their addresses is ignored. (This results in a normal bus cycle.) These registers are readable at any time, but their contents are never latched. Unreliable data may be read when the timer is in the run state.
5. The counter preload registers are readable and writable at any time and this occurs independently of any timer operation. No protection mechanisms are provided against ill-timed writes.
6. The input frequency to the 24-bit counter from the TIN pin or prescaler output must be between 0 and the input frequency at the CLK pin divided by 32 regardless of the configuration chosen.
7. For configurations in which the prescaler is used (with the CLK pin or TIN pin as an input), the contents of the counter preload register (CPR) is transferred to the counter the first time that the prescaler passes from $00 to $1F (rolls over) after entering the run state. Thereafter, the counter decrements or is loaded from the counter preload register when the prescaler rolls over.
8. For configurations in which the prescaler is not used, the contents of the counter preload registers are transferred to the counter on the first asserted edge of the TIN input after entering the run state. On subsequent asserted edges the counter decrements or is loaded from the counter preload registers.
9. The lowest value allowed in the counter preload register for use with the counter is $000001.

Timer Interrupt Acknowledge Cycles

Several conditions can be present when the timer interrupt acknowledge pin (TIACK) is asserted. These conditions affect the PI/T's response and the termination of the bus cycle (see Table 10).

PROGRAMMER'S MODEL

The internal accessible register organization is represented in Table 11. Address space within the address map is reserved for future expansion. Throughout the PI/T data sheet, the following conventions are maintained.

1. A read from a reserved location in the map results in a read from the 'null register'. The null register returns all zeros for data and results in a normal bus cycle. A write to one of these locations results in a normal bus cycle but no write occurs.
2. Unused bits of a defined register are denoted by '*' and are read as zeros.
3. Bits that are unused in the chosen mode/submode but are used in others, are denoted by 'X', and are readable and writable. Their content, however, is ignored in the chosen mode/submode.

Table 10 RESPONSE TO TIMER INTERRUPT ACKNOWLEDGE

PC3/TOUT Function	Response to Asserted $\overline{TIACK}$
PC3 – Port C Pin	No response No $\overline{DTACK}$
TOUT – Square Wave	No response No $\overline{DTACK}$
TOUT – Negated Timer Interrupt Request	No response. No $\overline{DTACK}$
TOUT – Asserted Timer Interrupt Request	Timer Interrupt Vector Contents $\overline{DTACK}$ Asserted

Preliminary

Table 11 PI/T REGISTER ADDRESSING ASSIGNMENTS

Register	Register Select Bits					Accessible	Affected by Reset	Affected by Read Cycle
	5	4	3	2	1			
Port General Control Register (PGCR)	0	0	0	0	0	R W	Yes	No
Port Service Request Register (PSRR)	0	0	0	0	1	R W	Yes	No
Port A Data Direction Register (PADDR)	0	0	0	1	0	R W	Yes	No
Port B Data Direction Register (PBDDR)	0	0	0	1	1	R W	Yes	No
Port C Data Direction Register (PCDDR)	0	0	1	0	0	R W	Yes	No
Port Interrupt Vector Register (PIVR)	0	0	1	0	1	R W	Yes	No
Port A Control Register (PACR)	0	0	1	1	0	R W	Yes	No
Port B Control Register (PBCR)	0	0	1	1	1	R W	Yes	No
Port A Data Register (PADR)	0	1	0	0	0	R W	No	* *
Port B Data Register (PBDR)	0	1	0	0	1	R W	No	* *
Port A Alternate Register (PAAR)	0	1	0	1	0	R	No	No
Port B Alternate Register (PBAR)	0	1	0	1	1	R	No	No
Port C Data Register (PCDR)	0	1	1	0	0	R W	No	No
Port Status Register (PSR)	0	1	1	0	1	R W*	Yes	No
Timer Control Register (TCR)	1	0	0	0	0	R W	Yes	No
Timer Interrupt Vector Register (TIVR)	1	0	0	0	1	R W	Yes	No
Counter Preload Register High (CPRH)	1	0	0	1	1	R W	No	No
Counter Preload Register Middle (CPRM)	1	0	1	0	0	R W	No	No
Counter Preload Register Low (CPRL)	1	0	1	0	1	R W	No	No
Count Register High (CNTRH)	1	0	1	1	1	R	No	No
Count Register Middle (CNTRM)	1	1	0	0	0	R	No	No
Count Register Low (CNTRL)	1	1	0	0	1	R	No	No
Timer Status Register (TSR)	1	1	0	1	0	R W*	Yes	No

*A write to this register may perform a special status resetting operation.
**Mode dependent.

R = Read
W = Write

4. All registers are addressable as 8-bit quantities. To facilitate operation with the MOVEP instruction and the DMAC, addresses are ordered such that certain sets of registers can also be accessed as words (2 bytes) or long words (4 bytes).

PORT GENERAL CONTROL REGISTER (PGCR)

The port general register controls many of the functions that are common to the overall operation of the ports. The PGCR is composed of three major fields: bits 7 and 6 define the operational mode of ports A and B and affect operation of the handshake pins and status bits; bits 5 and 4 allow a software controlled disabling of particular hardware associated with the handshake pins of each port; and bits 3-0 define the sense of the handshake pins. The PGCR is always readable and writable. All bits are reset to 0 when the RESET pin is asserted.

The port mode control field should be altered only when the H12 enable and H34 enable bits are 0. Except when mode 0 is desired, the port general control register must be written once to establish the mode, and again to enable the respective operation(s).

Port General Control Register (PGCR)

7	6	5	4	3	2	1	0
Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense

7 6 Port Mode Control
0 0 Mode 0 (unidirectional 8-Bit mode)
0 1 Mode 1 (unidirectional 16-bit mode)
1 0 Mode 2 (bidirectional 8-bit mode)
1 1 Mode 3 (bidirectional 16-bit mode)

5 H34 Enable
0 Disabled
1 Enabled

4 H12 Enable
0 Disabled
1 Enabled

3-0 Handshake Pin Sense
0 The associated pin is at the high voltage level when negated and at the low voltage level when asserted.
1 The associated pin is at the low voltage level when negated and at the high voltage level when asserted.

PORT SERVICE REQUEST REGISTER (PSRR)

The port service request register controls other functions that are common to the overall operation to the ports. It is composed of four major fields: bit 7 is unused and is always read as 0; bits 6 and 5 define whether interrupt or DMA requests are generated from activity on the H1 and H3

Preliminary

handshake pins; bits 4 and 3 determine whether two dual function pins operate as port C or port interrupt request/acknowledge pins; and bits 2, 1, and 0 control the priority among all port interrupt sources. Since bits 2, 1, and 0 affect interrupt operation, it is recommended that they be changed only when the affected interrupt(s) is disabled or known to remain inactive. The PSRR is always readable and writable.

All bits are reset to 0 when the RESET pin is asserted.

Port Service Request Register (PSRR)

7	6	5	4	3	2	1	0
*	SVCRQ Select		Interrupt PFS		Port Interrupt Priority Control		

6 5 SVCRQ Select

0 X The PC4/DMAREQ pin carries the PC4 function; DMA is not used.

1 0 The PC4/DMAREQ pin carries the DMAREQ function and is associated with double buffered transfers controlled by H1. H1 is removed from the PI/T's interrupt structure, and thus, does not cause interrupt requests to be generated. To obtain DMAREQ pulses, port A control register bit 1 (H1 SVCRQ enable) must be a 1.

1 1 The PC4/DMAREQ pin carries the DMAREQ function and is associated with double buffered transfers controlled by H3. H3 is removed from the PI/T's interrupt structure, and thus, does not cause interrupt requests to be generated. To obtain DMAREQ pulses, Port B Control Register bit 1 (H3 SVCRQ Enable) must be 1.

4 3 Interrupt Pin Function Select

0 0 The PC5/PIRQ pin carries the PC5 function.
The PC6/PIACK pin carries the PC6 function.

0 1 The PC5/PIRQ pin carries the PIRQ function.
The PC6/PIACK pin carries the PC6 function.

1 0 The PC5/PIRQ pin carries the PC5 function.
The PC6/PIACK pin carries the PIACK function.

1 1 The PC5/PIRQ pin carries the PIRQ function.
The PC6/PIACK pin carries the PIACK function.

Bits 2, 1, and 0 determine port interrupt priority. The priority is shown in descending order left to right.

Port Interrupt Priority Control

2 1 0	Highest			Lowest
0 0 0	H1S	H2S	H3S	H4S
0 0 1	H2S	H1S	H3S	H4S
0 1 0	H1S	H2S	H4S	H3S
0 1 1	H2S	H1S	H4S	H3S
1 0 0	H3S	H4S	H1S	H2S
1 0 1	H3S	H4S	H2S	H1S
1 1 0	H4S	H3S	H1S	H2S
1 1 1	H4S	H3S	H2S	H1S

PORT A DATA DIRECTION REGISTER (PADDR)

The port A data direction register determines the direction and buffering characteristics of each of the port A pins. One bit in the PADDR is assigned to each pin. A 0 indicates that the pin is used as an input, while a 1 indicates it is used as an output. The PADDR is always readable and writable. This register is ignored in mode 3.

All bits are reset to the 0 (input) state when the RESET pin is asserted.

PORT B DATA DIRECTION REGISTER (PBDDR)

The PBDDR is identical to the PADDR for the port B pins and the port B data register, except that this register is ignored in modes 2 and 3.

PORT C DATA DIRECTION REGISTER (PCDDR)

The port C data direction register specifies whether each dual function pin that is chosen for the port C operation is an input (0) or an output (1) pin. The PCDDR, along with bits that determine the respective pin's function, also specify the exact hardware to be accessed at the port C data register address. (See the Port C Data Register description for more details.) The PCDDR is an 8-bit register that is readable and writable at all times. Its operation is independent of the chosen PI/T mode.

These bits are cleared to 0 when the RESET pin is asserted.

PORT INTERRUPT VECTOR REGISTER (PIVR)

The port interrupt vector register contains the upper order six bits of the four port interrupt vectors. The contents of this register can be read two ways: by an ordinary read cycle, or by a port interrupt acknowledge bus cycle. The exact data read depends on how the cycle was initiated and other factors. Behavior during a port interrupt acknowledge cycle is summarized in Table 4.

Port Interrupt Vector Register (PIVR)

7	6	5	4	3	2	1	0
Interrupt Vector Number						*	*

From a normal read cycle (CS), there is never a consequence to reading this register. Following negation of the RESET pin, but prior to writing to the PIVR, a $0F will be read. After writing to the register, the upper 6 bits may be read and the lower 2 bits are forced to 0. No prioritization computation is performed.

PORT A CONTROL REGISTER (PACR)

The port A control register, in conjunction with the programmed mode and the port B submode, control the operation of port A and the handshake pins H1 and H2. The port A control register contains five fields: bits 7 and 6 specify the port A submode; bits 5, 4, and 3 control the operation of the H2 handshake pin and H2S status bit; bit 2 determines whether an interrupt will be generated when the H2S status bit goes to 1; bit 1 determines whether a service request (interrupt request or DMA request) will occur; bit 0 controls the operation of the H1S status bit. The PACR is always readable and writable.

All bits are cleared to 0 when the RESET pin is asserted. When the port A submode field is relevant in a mode/submode definition, it must not be altered unless the H12 enable bit in the port general control register is 0 (see Table 3).

The operation of H1 and H2 and their related status bits is given below for each of the modes specified by the port general control register bits 7 and 6.

Bits 2 and 1 carry the same meaning in each mode/submode, and thus are specified only once.

Port A Control Register (PACR)

7	6	5	4	3	2	1	0
Port A Submode		H2 Control			H2 Int Enable	H1 SVCRQ Enable	H1 Stat Ctrl

2 H2 Interrupt Enable

0 The H2 interrupt is disabled.

1 The H2 interrupt is enabled.

1 H1 SVCRQ Enable

0 The H1 interrupt and DMA request are disabled.

1 The H1 interrupt and DMA request are enabled.

Preliminary

Mode 0, Port A Submode 00

5 4 3 H2 Control
0 X X Input pin—status only.
1 0 0 Output pin—always negated.
1 0 1 Output pin—always asserted.
1 1 0 Output pin—interlocked input handshake protocol.
1 1 1 Output pin—pulsed input handshake protocol.

0 H1 Status Control
X Not used

Mode 0, Port A Submode 01

5 4 3 H2 Control
0 X X Input pin—status only.
1 0 0 Output pin—always negated.
1 0 1 Output pin—always asserted.
1 1 0 Output pin—interlocked output handshake protocol.
1 1 1 Output pin—pulsed output handshake protocol.

0 H1 Status Control
0 The H1S status bit is 1 when either the port A initial or final output latch can accept new data. It is 0 when both latches are full and cannot accept new data.
1 The H1S status bit is 1 when both of the port A output latches are empty. It is 0 when at least one latch is full.

Mode 0, Port A Submode 1X

5 4 3 H2 Control
0 X X Input pin—status only.
1 X 0 Output pin—always negated.
1 X 1 Output pin—always asserted.

0 H1 Status Control
X Not used.

Mode 1, Port A Submode XX, Port B Submode X0

5 4 3 H2 Control
0 X X Input pin—status only.
1 X 0 Output pin—always asserted.
1 X 1 Output pin—always asserted.

0 H1 Status Control
X Not used.

Mode 1 Port A Submode XX Port B Submode X1

5 4 3 H2 Control
0 X X Input pin—status only.
1 X 0 Output pin—always negated.
1 X 1 Output pin—always asserted.

0 H1 Status Control
X Not used.

Mode 2

5 4 3 H2 Control
X X 0 Output pin—interlocked output handshake protocol.
X X 1 Output pin—pulsed output handshake protocol.

0 H1 Status Control
0 The H1S status bit is 1 when either the port B initial or final output latch can accept new data. It is 0 when both latches are full and cannot accept new data.
1 The H1S status bit is 1 when both of the port B output latches are empty. It is 0 when at least one latch is full.

Mode 3

5 4 3 H2 Control
X X 0 Output pin—interlocked output handshake protocol.
X X 1 Output pin—pulsed output handshake protocol.

0 H1 Status Control
0 The H1S status bit is 1 when either the initial or final output latch of port A and B can accept new data. It is 0 when both latches are full and cannot accept new data.
1 The H1S status bit is 1 when both the initial and final output latches of ports A and B are empty. It is 0 when either the initial or final latch of ports A and B is full.

PORT B CONTROL REGISTER (PBCR)

The port B control register specifies the operation of port B and the handshake pins H3 and H4. The port B control register contains five fields: bits 7 and 6 specify the port B submode; bits 5, 4, and 3 control the operation of the H4 handshake pin and H4S status bit; bit 2 determines whether an interrupt will be generated when the H4S status bit goes to 1; bit 1 determines whether a service request (interrupt request or DMA request) will occur; bit 0 controls the operation of the H3S status bit. The PACR is always readable and writable. There is never a consequence to reading the register.

All bits are cleared to 0 when the RESET pin is asserted. When the port B submode field is relevant in a mode/submode definition, it must not be altered unless the H34 enable bit in the port general control register is 0 (see Table 3).

The operation of H3 and H4 and their related status bits is given below for each of the modes specified by the port general control register bits 7 and 6.

Bits 2 and 1 carry the same meaning in each mode/submode, and thus are specified only once.

Port B Control Register (PBCR)

7	6	5	4	3	2	1	0
Port B Submode		H4 Control			H4 Int Enable	H3 SVCRQ Enable	H3 Stat Ctrl

2 H4 Interrupt Enable
0 The H4 interrupt is disabled.
1 The H4 interrupt is enabled.

1 H3 SVCRQ Enable
0 The H3 interrupt and DMA request are disabled.
1 The H3 interrupt and DMA request are enabled.

Mode 0, Port B Submode 00

5 4 3 H4 Control
0 X X Input pin — status only.
1 0 0 Output pin — always negated.
1 0 1 Output pin — always asserted.
1 1 0 Output pin — interlocked input handshake protocol.
1 1 1 Output pin — pulsed input handshake protocol.

0 H3 Status Control
0 Not used.

Mode 0, Port B Submode 01

5 4 3 H4 Control
0 X X Input pin—status only.
1 0 0 Output pin—always negated.
1 0 1 Output pin—always asserted.
1 1 0 Output pin—interlocked output handshake protocol.
1 1 1 Output pin—pulsed output handshake protocol.

0 H3 Status Control
0 The H3S status bit is 1 when either the port B initial or final output latch can accept new data. It is 0 when both latches are full and cannot accept new data.
1 The H3S status bit is 1 when both of the port B output latches are empty. It is 0 when at least one latch is full.

Preliminary

Mode 0, Port B Submode 1X

5	4	3	H4 Control
0	X	X	Input pin—status only.
1	X	0	Output pin—always negated.
1	X	1	Output pin—always asserted.

0	H3 Status Control
X	Not used.

Mode 1, Port B Submode X0

5	4	3	H4 Control
0	X	X	Input pin—status only.
1	0	0	Output pin—always negated.
1	0	1	Output pin—always asserted.
1	1	0	Output pin—interlocked input handshake protocol.
1	1	1	Output pin—pulsed input handshake protocol.

0	H3 Status Control
X	Not used.

Mode 1, Port B Submode X1

5	4	3	H4 Control
0	X	X	Input pin—status only.
1	0	0	Output pin—always negated.
1	0	1	Output pin—always asserted.
1	1	0	Output pin—interlocked output handshake protocol.
1	1	1	Output pin—pulsed output handshake protocol.

0	H3 Status Control
0	The H3S status bit is 1 when either the initial or final output latch of port A and B can accept new data. It is 0 when both latches are full and cannot accept new data.
1	The H3S status bit is 1 when both the initial and final output latches of ports A and B are empty. It is 0 when neither the initial or final latch of ports A and B is full.

Mode 2

5	4	3	H4 Control
X	X	0	Output pin—interlocked input handshake protocol.
X	X	1	Output pin—pulsed input handshake protocol.

0	H3 Status Control
X	Not used.

Mode 3

5	4	3	H4 Control
X	X	0	Output pin—interlocked input handshake protocol.
X	X	1	Output pin—pulsed input handshake protocol.

0	H3 Status Control
X	Not used.

PORT A DATA REGISTER (PADR)

The port A data register is an address for moving data to and from the port A pins. The port A data direction register determines whether each pin is an input (0) or an output (1), and is used in configuring the actual data paths. PADR is mode dependent.

This register is readable and writable at all times. Depending on the chosen mode/submode, reading or writing may affect the double buffered handshake mechanism. The port A data register is not affected by the assertion of the RESET pin.

PORT B DATA REGISTER (PBDR)

The port B data register is an address for moving data to and from the port B pins. The port B data direction register determines whether each pin is an input (0) or an output (1), and is used in configuring the actual data paths. PBDR is mode dependent.

This register is readable and writable at all times. Depending on the chosen mode/submode, reading or writing may affect the double buffered handshake mechanism. The port B data register is not affected by the assertion of the RESET pin.

PORT A ALTERNATE REGISTER (PAAR)

The port A alternate register is an alternate address for reading the port A pins. It is a read only address and no other PI/T condition is affected. In all modes, the instantaneous pin level is read and no input latching is performed except at the data bus interface (see Bus Interface Connection). Writes to this address are answered with DTACK, but the data is ignored.

PORT B ALTERNATE REGISTER (PBAR)

The port B alternate register is an alternate address for reading the port B pins. It is a read only address and no other PI/T condition is affected. In all modes, the instantaneous pin level is read and no input latching is performed except at the data bus interface (see Bus Interface Connection). Writes to this address are answered with DTACK, but the data is ignored.

PORT C DATA REGISTER (PCDR)

The port C data register is an address for moving data to and from each of the eight port C/alternate function pins. The exact hardware accessed is determined by the type of bus cycle (read or write) and individual conditions affecting each pin. These conditions are: whether the pin is used for the port C or alternate function, and whether the port C data direction register indicates the input or output direction. The port C data register is singe buffered for output pins and not buffered for input pins. These conditions are summarized in table 12.

The Port C data register is not affected by the assertion of the RESET pin.

The operation of the PCDR is independent of the chosen PI/T mode.

Note that two additional useful benefits result from this structure. First, it is possible to directly read the state of a dual function pin while used for the non port C function. Second, it is possible to generate program controlled transitions on alternate function pins by switching back to the port C function, and writing to the PCDR.

This register is readable and writable at all times.

PORT STATUS REGISTER (PSR)

The port status register contains information about handshake pin activity. Bits 7-4 show the instantaneous level of the respective handshake pin, and is independent of the handshake pin sense bits in the port general control register. Bit 3-0

Table 12 PCDR HARDWARE ACCESSES

Read Port C Data Register			
Port C function PCDDR = 0	Port C function PCDDR = 1	Alternate function PCDDR = 0	Alternate function PCDDR = 1
pin	Port C output register	pin	Port C output register
Write Port C Data Register			
Port C function PCDDR = 0	Port C function PCDDR = 1	Alternate function PCDDR = 0	Alternate function PCDDR = 1
Port C output register, buffer disabled	Port C output register, buffer enabled	Port C output register	Port C output register

Preliminary

are the respective status bits referred to throughout this data sheet. Their interpretation depends on the programmed mode/submode of the PI/T. For bits 3-0, a 1 is the active or asserted state.

Port Status Register (PSR)

7	6	5	4	3	2	1	0
H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S

TIMER CONTROL REGISTER (TCR)

The timer control register determines all operations of the timer. Bits 7-5 configure the PC3/TOUT and PC7/TIACK pins for port C, square wave, vectored interrupt, or autovectored interrupt operation; bit 4 specifies whether the counter receives data from the counter preload register or continues counting when zero detect is reached; bit 3 is unused and is read as 0; bits 2 and 1 configure the path from the CLK and TIN pins to the counter controller; bit 0 enables the timer. This register is readable and writable at all times.

All bits are cleared to 0 when the RESET pin is asserted.

Timer Control Register (TCR)

7	6	5	4	3	2	1	0
TOUT/TIACK Control			Z D Ctrl	-	Clock Control		Timer Enable

7 6 5 TOUT/TIACK Control

0 0 X The dual function pins PC3/TOUT and PC7/TIACK carry the port C function.

0 1 X The dual function pin PC3/TOUT carries the TOUT function. In the run state it is used as a square wave output and is toggled on zero detect. The TOUT pin is high while in the halt state. The dual function pin PC7/TIACK carries the PC7 function.

1 0 0 The dual function pin PC3/TOUT carries the TOUT function. In the run or halt state it is used as a timer interrupt request output. The timer interrupt is disabled; thus, the pin is always three-stated. The dual function pin PC7/TIACK carries the TIACK function; however, since interrupt request is negated, the PI/T produces no response, i.e., no data or DTACK to an asserted TIACK. Refer to the Timer Interrupt Cycle section for details. This combination and the 101 state below support vectored timer interrupts.

1 0 1 The dual function pin PC3/TOUT carries the TOUT function and is used as a timer interrupt request output. The timer interrupt is enabled; thus, the pin is low when the timer ZDS status bit is 1. The dual function pin PC7/TIACK carries the TIACK function and is used as a timer interrupt acknowledge input. Refer to the Timer Interrupt Acknowledge Cycle section for details. This combination and the 100 state above support vectored timer interrupts.

1 1 0 The dual function pin PC3/TOUT carries the TOUT function. In the run or halt state it is used as a timer interrupt request output. The timer interrupt is disabled; thus, the pin is always three-stated. The dual function pin PC7/TIACK carries the PC7 function.

1 1 1 The dual function pin PC3/TOUT carries the TOUT function and is used as a timer interrupt request output. The timer interrupt is enabled; thus, the pin is low when the timer ZDS status bit is 1. The dual function pin PC7/TIACK carries the PC7 function and autovectored interrupts are supported.

4 Zero Detect Control

0 The counter is loaded from the counter preload register on the first clock to the 24-bit counter after zero detect, and resumes counting.

1 The counter rolls over on zero detect, then continues counting.

Bit 3 is unused and is always read as 0.

2 1 Clock Control

0 0 The PC2/TIN input pin carries the port C function and the CLK pin and prescaler are used. The prescaler is decremented on the falling transition of the CLK pin; the 24-bit counter is decremented or loaded from the counter preload registers when the prescaler rolls over from $00 to $1F. The timer enable bit determines whether the timer is in the run or halt state.

0 1 The PC2/TIN pin serves as a timer input and the CLK pin and prescaler are used. The prescaler is decremented on the falling transition of the CLK pin; the 24-bit counter is decremented or loaded from the counter preload registers when the prescaler rolls over from $00 to $1F. The timer is in the run state when the timer enable bit is 1 and the TIN pin is high; otherwise the timer is in the halt state.

1 0 The PC2/TIN pin serves as a timer input and the prescaler is used. The prescaler is decremented following the rising transition of the TIN pin after syncing with the internal clock. The 24-bit counter is decremented or loaded from the counter preload registers when the prescaler rolls over from $00 to $1F. The timer enable bit determines whether the timer is in the run or halt state.

1 1 The PC2/TIN pin serves as a timer input and the prescaler is unused. The 24-bit counter is decremented or loaded from the counter preload registers following the rising edge of the TIN pin after syncing with the internal clock. The timer enable bit determines whether the timer is in the run or halt state.

0 Timer Enable

0 Disabled.

1 Enabled.

TIMER INTERRUPT VECTOR REGISTER (TIVR)

The timer interrupt vector register contains the 8-bit vector supplied when the timer interrupt acknowledge pin TIACK is asserted. The register is readable and writable at all times, and the same value is always obtained from a normal read cycle and a timer interrupt acknowledge bus cycle (TIACK). When the RESET pin is asserted, the value of $0F is automatically loaded into the register. Refer to the Timer Interrupt Acknowledge Cycle section for more details.

COUNTER PRELOAD REGISTER H, M, L (CPRH-L)

The counter preload registers are a group of three 8-bit registers used for storing data to be transferred to the counter. Each of the registers is individually addressable, or the group may be accessed with the MOVEP.L or the MOVEP.W instructions. The address one less than the address of CPRH is the null register, and is reserved so that zeros are read in the upper 8 bits of the destination data register when a MOVEP.L is used. Data written to this address is ignored.

Preliminary

The registers are readable and writable at all times. A read cycle proceeds independently of any transfer to the counter, which may be occurring simultaneously.

To insure proper operation of the PI/T timer, a value of $000000 cannot be stored in the counter preload registers for use with the counter.

The RESET pin does not affect the contents of these registers.

Counter Preload Register H, M, L (CPRH-L)

7	6	5	4	3	2	1	0	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	CPRH
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	CPRM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CPRL

COUNT REGISTER H, M, L (CNTRH-L)

The count registers are a group of three 8-bit addresses at which the counter can be read. The contents of the counter are not latched during a read bus cycle; thus, the data read at these addresses is not guaranteed if the timer is in the run state. (Bits 2, 1 and 0 of the timer control register specify the state.) Write operations to these addresses result in a normal bus cycle but the data is ignored.

Each of the registers is individually addressable, or the group can be accessed with the MOVEP.L or the MOVEP.W instructions. The address one less than the address of CNTRH is the null register, and is reserved so that zeros are read in the upper 8 bits of the destination data register when a MOVEP.L is used. Data written to this address is ignored.

Count Register H, M, L (CNTRH-L)

7	6	5	4	3	2	1	0	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	CNTRH
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	CNTRM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CNTRL

TIMER STATUS REGISTER (TSR)

The timer status register contains one bit from which the zero detect status can be determined. The ZDS status bit (bit 0) is an edge sensitive flip flop that is set to 1 when the 24-bit counter decrements from $000001 to $000000. The ZDS status bit is cleared to 0 following the direct clear operation (similar to that of the ports), or when the timer is halted. Note also that when the RESET pin is asserted, the timer is disabled and thus enters the halt state.

This register is always readable without consequence. A write access performs a direct clear operation if bit 0 in the written data is 1. Following that, the ZDS bit is 0.

This register is constructed with a reset dominant S-R flip flop so that all clearing conditions prevail over the possible zero detect condition.

Bits 7-1 are unused and are read as 0.

Timer Status Register (TSR)

7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	ZDS

TIMER APPLICATIONS SUMMARY

Periodic Interrupt Generator

In this configuration the timer generates a periodic interrupt. The TOUT pin is connected to the system's interrupt request circuitry and the TIACK pin can be used as an interrupt acknowledge input to the timer. The TIN pin can be used as a clock input.

The processor loads the counter preload registers and timer control register, and then enables the timer. When the 24-bit counter passes from $000001 to $000000, the ZDS status bit is set and the TOUT (interrupt request) pin is asserted. At the next clock to the 24-bit counter, it is again loaded with the contents of the CPRs and thereafter decrements. In normal operation, the processor must direct clear the status bit to negate the interrupt request (see Figure 8).

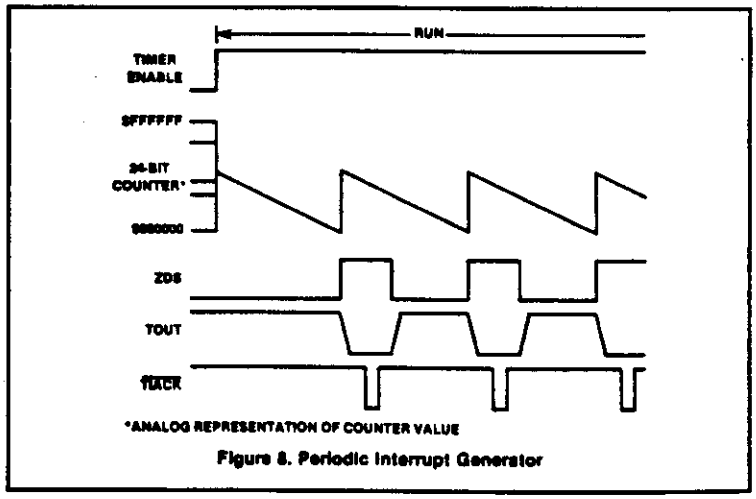
Periodic Interrupt Generator

7	6	5	4	3	2	1	0
TOUT, TIACK Control			Z D Ctrl	*	Clock Control		Timer Enable
1	X	1	0	0	00 or 1X		changed

Square Wave Generator

In this configuration the timer produces a square wave at the TOUT pin. The TOUT pin is connected to the user's circuitry and the TIACK pin is not used. The TIN pin may be used as a clock input.

The processor loads the counter preload registers and timer control register, and then enables the timer. When the 24-bit counter passes from $000001 to $000000, the ZDS status bit is set and the TOUT (square wave output) pin is toggled. At the next clock to the 24-bit counter, it is again loaded with the contents of the CPRs and thereafter decrements. In this application there is no need for the processor to direct clear the ZDS status bit; however, it is possible for the processor to sync itself with the square wave by clearing the ZDS status bit, then polling it. The processor can also read the TOUT level at the port C address.



*ANALOG REPRESENTATION OF COUNTER VALUE

Figure 8. Periodic Interrupt Generator

Preliminary

Note that the PC3/TOUT pin functions as PC3 following the negation of RESET. If used in the square wave configuration, a pullup resistor may be required to keep a known level prior to programming. Prior to enabling the timer, TOUT is high (see Figure 9).

Square Wave Generator

7	6	5	4	3	2	1	0
TOUT/TIACK Control			Z D Ctl	*	Clock Control		Timer Enable
0	1	X	0	0	00 or 1X		changed

Interrupt After Timeout

In this configuration the timer generates an interrupt after a programmed time period has expired. The TOUT pin is connected to the system's interrupt request circuitry and the TIACK pin can be an interrupt acknowledge input to the timer. The TIN pin may be used as a clock input.

This configuration is similar to the periodic interrupt generator except that the zero detect control bit is set. This forces the counter to roll over after zero detect is reached, rather than reloading from the CPRs. When the processor takes the interrupt, it can halt the timer and read the counter. This allows the processor to measure the delay time from zero detect (interrupt request) to entering the service routine. Accurate knowledge of the interrupt latency may be useful in some applications (see Figure 10).

Interrupt After Timeout

7	6	5	4	3	2	1	0
TOUT/TIACK Control			Z D Ctl	*	Clock Control		Timer En
1	X	1	1	0	00 or 1X		changed

Elapsed Time Measurement

Elapsed time measurement takes several forms; two are described below. The first configuration allows time interval measurement by software. No timer pins are used.

The processor loads the counter preload registers (generally with all 1s) and timer control register, and then enables the timer. The counter decrements until the ending event takes place. When it is desired to read the time interval, the processor must halt the timer, then read the counter. For applications in which the interval could have exceeded that programmable in this timer, interrupts can be counted to provide the equivalent of additional timer bits. At the end, the timer can be halted and read (see Figure 11).

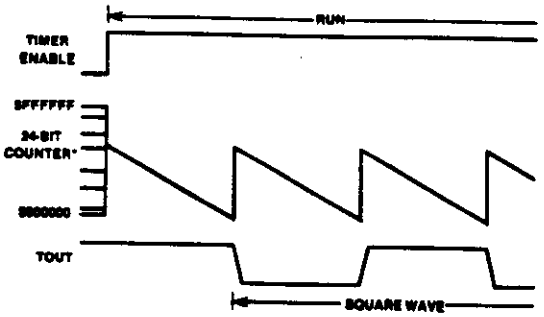


Figure 9. Square Wave Generator

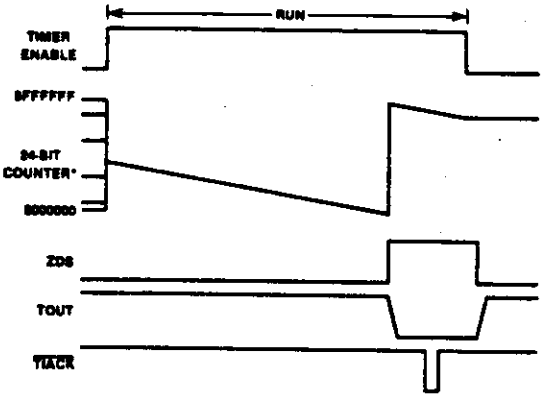


Figure 10. Single Interrupt After Timeout

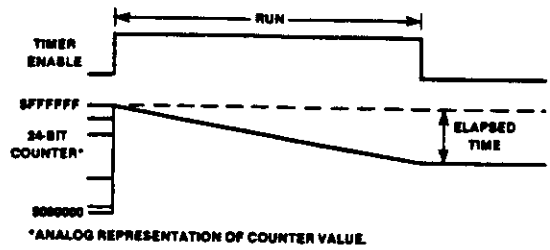


Figure 11. Elapsed Time Measurement

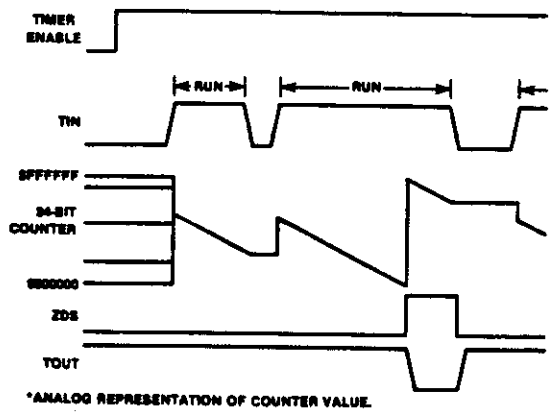


Figure 12. Device Watchdog

System Clock

7	6	5	4	3	2	1	0
TOUT/TIACK Control			Z D Ctrl	*	Clock Control		Timer Enable
0	0	X	1	0	0	0	changed

The second configuration allows measurement (counting) of the number of input pulses occurring in an interval in which the counter is enabled. The TIN input pin provides the input pulses. Generally the TOUT and TIACK pins are not used.

This configuration is identical to the elapsed time measurement/system clock configuration except that the TIN pin is used to provide the input frequency. It can be connected to a simple oscillator, and the same methods could be used. Alternately, it could be gated off and on externally and the number of cycles occurring while in the run state can be counted. However, minimum pulse width high and low specifications must be met.

External Clock

7	6	5	4	3	2	1	0
TOUT/TIACK Control			Z D Ctrl	*	Clock Control		Timer Enable
0	0	X	1	0	1	X	changed

Device Watchdog

This configuration provides the watchdog function needed in many systems. The TIN pin is the timer input whose period at the high (1) level is to be checked. Once allowed by the processor, the TIN input pin controls the run/halt mode. The TOUT pin is connected to external circuitry requiring notification when the TIN pin has been asserted longer than the programmed time. The TIACK pin (interrupt acknowledge) is only needed if the TOUT pin is connected to interrupt circuitry.

The processor loads the counter preload register and timer control register, and then enables the timer. When the TIN input is asserted (1, high) the timer transfers the contents of the counter preload register to the counter and begins counting. If the TIN input is negated before zero detect is reached, the TOUT output and the ZDS status bit remain negated. If zero detect is reached while the TIN input is still asserted, the ZDS status bit is set and the TOUT output is asserted. (The counter rolls over and keeps on counting).

In either case, when the TIN input is negated, the ZDS status bit is 0, the TOUT output is negated, the counting stops, and prescaler is forced to all is (see Figure 12).

Preliminary

Device Watchdog

7	6	5	4	3	2	1	0
TOUT/TIACK Control			Z D Ctrl	*	Clock Control		Timer Enable
1	X	1	1	0	0	1	changed

BUS INTERFACE CONNECTION

The PI/T has an asynchronous bus interface, primarily designed for use with the SCN68000 microprocessor. With care, however, it can be connected to asynchronous microprocessor buses. This section completely describes the PI/T's bus interface, and is intended for the asynchronous bus designer unless otherwise specified.

In an asynchronous system, the PI/T CLK can operate at a significantly different frequency, either higher or lower than the bus master and other system components, as long as all bus specifications are met. The SCN68230 CLK pin has the same specifications as the SCN68000 CLK, and must not be gated off at any time.

The following signals generate normal read and write cycles to the PI/T: CS (chip select), R/W (read/write), RS1-RS5 (five register select bits), D0-D7 (the 8-bit bidirectional data bus), and DTACK (data transfer acknowledge). To generate interrupt acknowledge cycles, PC6/PIACK or PC7/TIACK is used instead of CS and the register select pins are ignored. No combination of the following pins can be asserted simultaneously: CS, PIACK, or TIACK.

Read Cycles via Chip Select

This category includes all register reads, except port or timer interrupt acknowledge cycles. When CS is asserted, the register select and R/W inputs are latched internally. They must meet small setup and hold time requirements with respect to the asserted edge of CS (see the AC Electrical Characteristics table). The PI/T is not protected against aborted (shortened) bus cycles generated by an address error or bus error exception in which it is addressed.

Certain operations triggered by normal read (or write) bus cycles are not complete within the time allotted to the bus cycle. One example is transfers to/from the double buffered latches that occur as a result of the bus cycle. If the bus master's CLK is significantly faster than the PI/T's, the possibility exists that, following the bus cycle, CS can be negated then reasserted before completion of these internal operations. In this situation the PI/T does not recognize the reassertion of CS until these operations are complete. Only at that time does it begin the internal sequencing necessary to react to the asserted CS. Since CS also controls the DTACK response, this 'bus cycle recovery time' can be related to the CLK edge on which DTACK is asserted for that cycle. The PI/T will recognize the subsequent assertion of CS three CLK periods after the CLK edge on which DTACK was previously asserted.

The register select and R/W inputs pass through an internal latch that is transparent when the PI/T can recognize a new CS pulse (see above paragraph). Since the internal data bus of the PI/T is continuously enabled for read transfers, the read access time (to the data bus buffers) begins when the register selects are stabilized internally. Also, when the PI/T is ready to begin a new bus cycle, the assertion of CS enables the data bus buffers within a short propagation delay. This does not contribute to the overall read access time, unless CS is asserted significantly after the register select and R/W inputs are stabilized (as may occur with synchronous bus microprocessors).

In addition to chip select's previously mentioned duties, it controls the assertion of DTACK and latching of read data at the data bus interface. Except for controlling input latches and enabling the data bus buffers, all of these functions occur only after CS has been recognized internally and synchronized with the internal clock. Chip select is recognized on the falling edge of the CLK if the setup time is met, and DTACK is asserted (low) on the next falling edge of the CLK. Read data is latched at the PI/T's data bus interface at the same time DTACK is asserted. It is stable as long as chip select remains asserted independent of other external conditions.

From the above discussion, it is clear that if the CS setup time prior to the falling edge of the CLK is met the PI/T can consistently respond to a new read or write bus cycle every four CLK cycles. This fact is especially useful in designing the PI/T's clock in synchronous bus systems not using DTACK. (An extra CLK period is required in interrupt acknowledge cycles, see Read Cycles via Interrupt Acknowledge).

In asynchronous bus systems in which the PI/T's CLK differs from that of the bus master, generally there is no way to guarantee that the CS setup time with respect to the PI/T CLK is met. Thus, the only way to determine that the PI/T recognized the assertion of CS is to wait for the assertion of DTACK. In this situation, all latched bus inputs to the PI/T must be held stable until DTACK is asserted. These include register select, R/W, and write data inputs (see below).

System specifications impose a maximum delay from the trailing (negated) edge of chip select to the negated edge of DTACK. As system speeds increase, this becomes more difficult to meet with a simple pullup resistor tied to the DTACK line. Therefore, the PI/T provides an internal active pullup device to reduce the rise time, and a level sensitive circuit that later turns this device off. DTACK is negated asynchronously as fast as possible following the rising edge of chip select, then three-stated to avoid interference with the next bus cycle.

The system designer must take care that DTACK is negated and three-stated quickly enough after each bus cycle to avoid interference with the next one. With the SCN68000 this necessitates a relatively fast external path from the data strobe to CS going negated.

Write Cycles

In many ways write cycles are similar to normal read cycles (see above). On write cycles, data at the D0-D7 pins must meet the same setup specifications as the register select and R/W lines. Like these signals, write data is latched on the asserted edge of CS, and must meet small setup and hold time requirements with respect to that edge. The same bus cycle recovery conditions exist as for normal read cycles. No other differences exist.

Read Cycles via Interrupt Acknowledge

Special internal operations take place on PI/T interrupt acknowledge cycles. The port interrupt vector register or the timer interrupt vector register are implicitly addressed by the assertion of PC6/PIACK or PC7/TIACK, respectively. The signals are first synchronized with the falling edge of the CLK. One clock period after they are recognized, the data bus buffers are enabled and the vector is driven onto the bus. DTACK is asserted after another clock period to allow the vector some setup prior to DTACK. DTACK is negated, then three-stated as with the normal read or write cycle when PIACK or TIACK is negated.

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER (DUART) SCN68681

Preliminary

DESCRIPTION

The Signetics SCN68681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It is compatible with other S68000 family devices, and can also interface easily with other microprocessors. The DUART can be used in polled or interrupt driven systems.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16x clock derived from a programmable counter/timer, or an external 1x or 16x clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

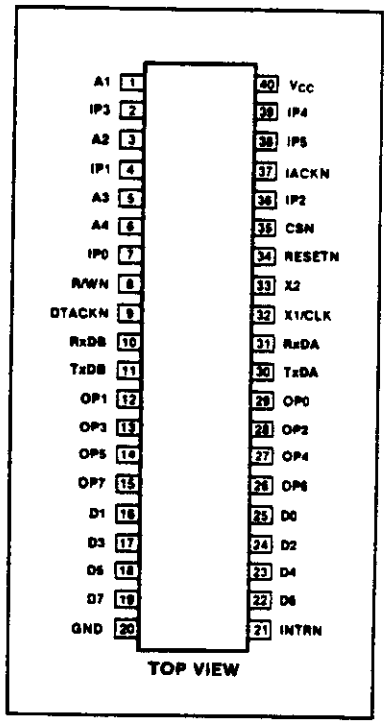
Each receiver is quadruply buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

Also provided on the SCN68681 are a multipurpose 6-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

FEATURES

- S68000 bus compatible
- Dual full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data registers
- Programmable data format
  - —5 to 8 data bits plus parity
  - —Odd, even, no parity or force parity
  - —1, 1.5 or 2 stop bits programmable in 1/16 bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - —18 fixed rates: 50 to 38.4K baud
  - —One user defined rate derived from programmable timer/counter
  - —External 1x or 16x clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - —Normal (full duplex)
  - —Automatic echo
  - —Local loopback
  - —Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 6-bit input port
  - —Can serve as clock or control inputs
  - —Change of state detection on four inputs
- Multi-function 8-bit output port
  - —Individual bit set/reset capability
  - —Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - —Single interrupt output with eight maskable interrupting conditions
  - —Interrupt vector output on interrupt acknowledge
  - —Output port can be configured to provide a total of up to six separate wire-OR'able interrupt outputs
- Maximum data transfer: 1X — 1MB/sec, 16X — 125KB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply

PIN CONFIGURATION



TOP VIEW

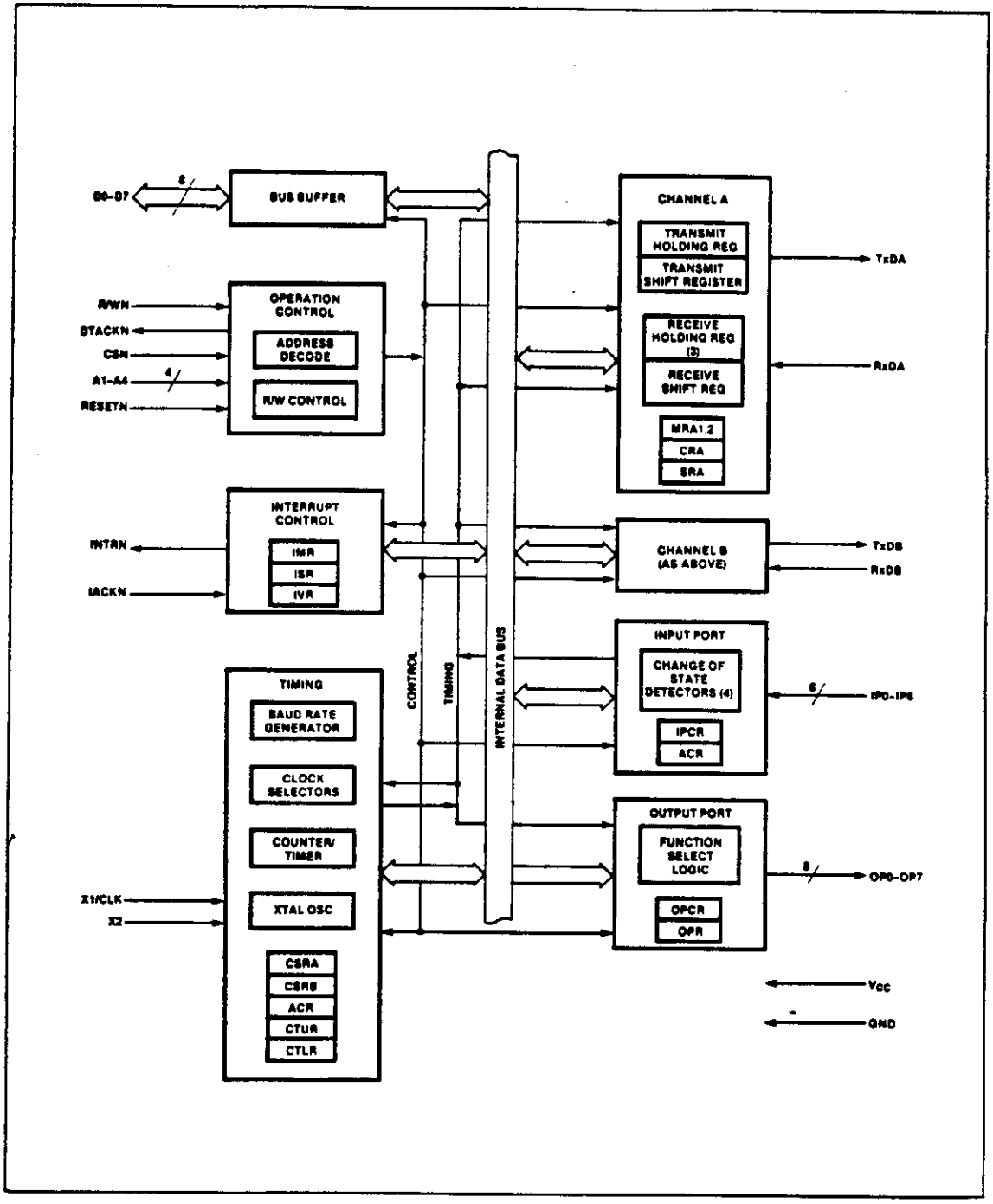
ORDERING CODE

PACKAGES	V_{CC} = 5V ± 5%, T_A = 0°C to 70°C
Ceramic DIP	SCN68681C1I40
Plastic DIP	SCN68681C1N40

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER (DUART) SCN68681

Preliminary

BLOCK DIAGRAM



DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER (DUART) SCN68681

Preliminary

PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
D0–D7	25–22, 16–19	I/O	**Data Bus:** Bidirectional 3-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	35	I	**Chip Select:** Active low input signal. When low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the R/WN and A1–A4 inputs. When high, places the D0–D7 lines in the 3-state condition.
R/WN	8	I	**Read/Write:** A high input indicates a read cycle and a low input indicates a write cycle, when a cycle is initiated by assertion of the CSN input.
A1–A4	1, 3, 5, 6	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESETN	34	I	**Reset:** A low clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to hex 0F, puts OP0–OP7 in the high state, stops the counter/timer, and puts channel A and B in the inactive state, with the TxDA and TxDB outputs in the mark (high) state.
DTACKN	9	O	**Data Transfer Acknowledge:** Three-state active low output asserted in write, read, or interrupt cycles to indicate proper transfer of data between the CPU and the DUART.
INTRN	21	O	**Interrupt Request:** Active low, open drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
IACKN	37	I	**Interrupt Acknowledge:** Active low input indicating an interrupt acknowledge cycle. In response, the DUART will place the interrupt vector on the data bus and will assert DTACKN if it has an interrupt pending.
X1/CLK	32	I	Crystal 1: Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. If a crystal is used, a capacitor must be connected from this pin to ground (see figure 7).
X2	33	I	**Crystal 2:** Connection for other side of the crystal. Should be connected to ground if a crystal is not used. If a crystal is used, a capacitor must be connected from this pin to ground (see figure 7).
RxDA	31	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
RxDB	10	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
TxDA	30	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
TxDB	11	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
OP0	29	O	**Output 0.** General purpose output, or channel A request to send (RTSAN, active low). Can be deactivated automatically on receive or transmit.
OP1	12	O	**Output 1:** General purpose output, or channel B request to send (RTSBN, active low). Can be deactivated automatically on receive or transmit.
OP2	28	O	**Output 2:** General purpose output, or channel A transmitter 1X or 16X clock output, or channel A receiver 1X clock output.
OP3	13	O	**Output 3:** General purpose output, or open drain, active low counter/timer output, or channel B transmitter 1X clock output, or channel B receiver 1X clock output.
OP4	27	O	**Output 4:** General purpose output, or channel A open drain, active low, RxRDYA/FFULLA output.

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER (DUART) SCN68681

Preliminary

PIN DESIGNATION (Continued)

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
OP5	14	O	Output 5: General purpose output, or channel B open drain, active low, RxRDYB/FFULLB output.
OP6	26	O	Output 6: General purpose output, or channel A open drain, active low, TxRDYA output.
OP7	15	O	Output 7: General purpose output, or channel B open drain, active low, TxRDYB output.
IP0	7	I	Input 0: General purpose input, or channel A clear to send active low input (CTSAN).
IP1	4	I	Input 1: General purpose input, or channel B clear to send active low input (CTSBN).
IP2	36	I	Input 2: General purpose input, or channel B receiver external clock input (RxCB), or counter/timer external clock input. When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP3	2	I	Input 3: General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	39	I	Input 4: General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	38	I	Input 5: General purpose input, or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V_{CC}	40	I	Power Supply: +5V supply input.
GND	20	I	Ground

BLOCK DIAGRAM

The SCN68681 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications channels A and B, input port and output port. Refer to the block diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data busses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The DTACKN output is asserted during write and read cycles to indicate to the CPU that data has been latched on a write cycle, or that valid data is present on the bus on a read cycle.

Interrupt Control

A single active low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the interrupt mask register (IMR), the interrupt status register (ISR), the auxiliary control register (ACR), and the interrupt vector register (IVR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. When IACKN is asserted, and the DUART has an interrupt pending, the DUART responds by placing the contents of the IVR register on the data bus and asserting DTACKN.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitters, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or an external timing signal.

The counter/timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER (DUART) SCN68681

Preliminary

Communications Channels A and B

Each communications channel of the SCN68681 comprises a full duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

Input Port

The inputs to this unlatched 6-bit port can be read by the CPU by performing a read operation at address D_{16}. A high input results in a logic 1 while a low input results in a logic 0. D7 will always be read as a logic 1 and D6 will reflect the level of IACKN. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1, and IP0. A high-to-low or low-to-high transition of these inputs lasting longer than 25–50μs will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change of state can also be programmed to generate an interrupt to the CPU.

Output Port

The 8-bit multi-purpose output port can be used as a general purpose output port, in which case the outputs are the complements of the output port register (OPR). OPR[n] = 1 results in OP[n] = low and vice-versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address E_{16} with the accompanying data specifying the bits to be set (1 = set, 0 = no change). Likewise, a bit is reset by a write at address F_{16} with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the channel A mode registers (MR1A, MR2A), the channel B mode registers (MR1B, MR2B), and the output port configuration register (OPCR).

OPERATION

Transmitter

The SCN68681 is conditioned to transmit data when the transmitter is enabled through the command register. The SCN68681 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the transmit holding register (THR), the above conditions are negated. Data is transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains high and the TxEMT bit in the status register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR. If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enabled, the CTSN input must be low in order for the character to be transmitted. If it goes high in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SCN68681 is conditioned to receive data when enabled through the command register. The receiver looks for a high to low (mark to space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled high, the start bit is invalid and the search for a valid start bit begins again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and the parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the receive holding register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, overrun error and received break state (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a high condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a first-in-first-out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the

data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit (SR[4]) will be set upon receipt of the start bit of the new (overruning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Multidrop Mode

The DUART is equipped with a wake up mode used for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for channels A and B respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wake-up' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, an address/data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data, while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to table 2 for register bit descriptions.

Table 1 68681 REGISTER ADDRESSING

A4	A3	A2	A1	READ (R/WN = 1)	WRITE (R/WN = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Reg. A (CSRA)
0	0	1	0	*Reserved*	Command Register A (CRA)
0	0	1	1	RX Holding Register A (RHRA)	TX Holding Register A (THRA)
0	1	0	0	Input Port Change Reg. (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Reg. (ISR)	Interrupt Mask Reg. (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CTUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Reg. B (CSRB)
1	0	1	0	*Reserved*	Command Register B (CRB)
1	0	1	1	RX Holding Register B (RHRB)	TX Holding Register B (THRB)
1	1	0	0	Interrupt Vector Reg. (IVR)	Interrupt Vector Reg. (IVR)
1	1	0	1	Input Port	Output Port Conf. Reg. (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

Preliminary

Table 2 REGISTER BIT FORMATS

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	RX RTS CONTROL	RX INT SELECT	ERROR MODE	PARITY MODE		PARITY TYPE	BITS PER CHAR.	
MR1A MR1B	0 = no 1 = yes	0 = RXRDY 1 = FFULL	0 = char 1 = block	00 = with parity 01 = force parity 10 = no parity 11 = multi-drop mode		0 = even 1 = odd	00 = 5 01 = 6 10 = 7 11 = 8	

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	CHANNEL MODE		Tx RTS CONTROL	CTS ENABLE Tx	STOP BIT LENGTH*			
MR2A MR2B	00 = Normal 01 = Auto echo 10 = Local loop 11 = Remote loop		0 = no 1 = yes	0 = no 1 = yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

*Add 0.5 to values shown for 0-7 if channel is programmed for 5 bits/char

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	RECEIVER CLOCK SELECT				TRANSMITTER CLOCK SELECT			
CSRA CSRB	See text				See text			

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	not used— must be 0	MISCELLANEOUS COMMANDS			DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
CRA CRB		See text			0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	RECEIVED BREAK	FRAMING ERROR	PARITY ERROR	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
SRA SRB	0 = no 1 = yes *	0 = no 1 = yes *	0 = no 1 = yes *	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

*These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits (7:5) from the top of the FIFO together with bits 4:0. These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	OP7	OP6	OP5	OP4	OP3		OP2	
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB (1X) 11 = RxCB (1X)		00 = OPR[2] 01 = TxCA (16X) 10 = TxCA (1X) 11 = RxCA (1X)	

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE			DELTA IP3 INT	DELTA IP2 INT	DELTA IP1 INT	DELTA IP0 INT
ACR	0 = set1 1 = set2	See table 4			0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	DELTA IP3	DELTA IP2	DELTA IP1	DELTA IP0	IP3	IP2	IP1	IP0
IPCR	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = low 1 = high	0 = low 1 = high	0 = low 1 = high	0 = low 1 = high

Preliminary

Table 2 REGISTER BIT FORMATS (Continued)

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ISR	INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IMR	IN. PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTUR	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTLR	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IVR	IVR[7]	IVR[6]	IVR[5]	IVR[4]	IVR[3]	IVR[2]	IVR[1]	IVR[0]

MR1A — Channel A Mode Register 1

MR1A is accessed when the channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] — Channel A Receiver Request-to-Send Control — This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] — Channel A Receiver Interrupt Select — This bit selects either the channel A receiver ready status (RXRDY) or the channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] — Channel A Error Mode Select — This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break) for channel A. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these bits is the accumulation (logical OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for channel A was issued.

MR1A[4:3] — Channel A Parity Mode Select — If 'with parity' or 'force parity' is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1A[4:3] = 11 selects channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] — Channel A Parity Type Select — This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] — Channel A Bits per Character Select — This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

Preliminary

MR2A — Channel A Mode Register 2

MR2A is accessed when the channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] — Channel A Mode Select — Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held high.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity bit is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected, the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop bit has been retransmitted.

MR2A[5] — Channel A Transmitter Request-to-Send Control — This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 causes OPR[0] to be reset automatically one bit time after the characters in the channel A transmit shift register and in the THR, if any, are completely transmitted, including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Assert RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

MR2A[4] — Channel A Clear-to-Send Control — If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IP0) each time it is ready to send a character. If IP0 is asserted (low), the character is transmitted. If it is negated (high), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character.

MR2A[3:0] — Channel A Stop Bit Length Select — This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled) in all cases.

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR1B — Channel B Mode Register 1

MR1B is accessed when the channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to the bit definitions for MR1A, except that all control actions apply to the channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B — Channel B Mode Register 2

MR2B is accessed when the channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for this register are identical to the bit definitions for MR2A, except that all control actions apply to the channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA — Channel A Clock Select Register

CSRA[7:4] — Channel A Receiver Clock Select — This field selects the baud rate clock for the channel A receiver as follows:

Preliminary

CSRA[7:4]	Baud Rate Clock = 3.6864MHz ACR[7] = 0	ACR[7] = 1
0 0 0 0	50	75
0 0 0 1	110	110
0 0 1 0	134.5	134.5
0 0 1 1	200	150
0 1 0 0	300	300
0 1 0 1	600	600
0 1 1 0	1,200	1,200
0 1 1 1	1,050	2,000
1 0 0 0	2,400	2,400
1 0 0 1	4,800	4,800
1 0 1 0	7,200	1,800
1 0 1 1	9,600	9,600
1 1 0 0	38.4K	19.2K
1 1 0 1	Timer	Timer
1 1 1 0	IP4—16X	IP4—16X
1 1 1 1	IP4—1X	IP4—1X

The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

CSRA[3:0] — Channel A Transmitter Clock Select — This field selects the baud rate clock for the channel A transmitter. The field definition is as per CSRA[7:4] except as follows:

CSRA[3:0]	Baud Rate ACR[7] = 0	ACR[7] = 1
1 1 1 0	IP3—16X	IP3—16X
1 1 1 1	IP3—1X	IP3—1X

The transmitter clock is always a 16X clock except for CSRA[3:0] = 1111.

CSRB — Channel B Clock Select Register

CSRB[7:4] — Channel B Receiver Clock Select — This field selects the baud rate clock for the channel B receiver. The field definition is as per CSRA[7:4] except as follows:

CSRB[7:4]	Baud Rate ACR[7] = 0	ACR[7] = 1
1 1 1 0	IP2—16X	IP2—16X
1 1 1 1	IP2—1X	IP2—1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] — Channel B Transmitter Clock Select — This field selects the baud rate clock for the channel B transmitter. The field definition is as per CSRA[7:4] except as follows:

CSRB[3:0]	Baud Rate ACR[7] = 0	ACR[7] = 1
1 1 1 0	IP5—16X	IP5—16X
1 1 1 1	IP5—1X	IP5—1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA — Channel A Command Register

CRA is a register used to supply commands to channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[6:4] — Channel A Miscellaneous Commands — The encoded value of this field may be used to specify a single command as follows:

CRA[6:4]	COMMAND
0 0 0	No command.
0 0 1	Reset MR pointer. Causes the channel A MR pointer to point to MR1.
0 1 0	Reset receiver. Resets the channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
0 1 1	Reset transmitter. Resets the channel A transmitter as if a hardware reset had been applied.
1 0 0	Reset error status. Clears the channel A Received Break, Parity Error, Framing Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.
1 0 1	Reset channel A break change interrupt. Causes the channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.
1 1 0	Start break. Forces the TXDA output low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any others loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.
1 1 1	Stop Break. The TXDA line will go high (marking) within two bit times. TXDA will remain high for one bit time before the next character, if any, is transmitted.

CRA[3] — Disable Channel A Transmitter — This command terminates transmitter operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] — Enable Channel A Transmitter — Enables operation of the channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] — Disable Channel A Receiver — This command terminates operation of the receiver immediately — a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] — Enable Channel A Receiver — Enables operation of the channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

CRB — Channel B Command Register

CRB is a register used to supply commands to channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, except that all control actions apply to the channel B receiver and transmitter and the corresponding inputs and outputs.

SRA — Channel A Status Register

SRA[7] — Channel A Received Break — This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half a bit time (two successive edges of the internal or external 1x clock).

When this bit is set, the channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] — Channel A Framing Error — This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] — Channel A Parity Error — This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the received A/D bit.

SRA[4] — Channel A Overrun Error — This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] — Channel A Transmitter Empty (TxEMTA) — This bit will be set when the channel A transmitter underruns, i.e., both the transmit holding register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

SRA[2] — Channel A Transmitter Ready (TxRDYA) — This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, viz., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] — Channel A FIFO Full (FFULLA) — This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] — Channel A Receiver Ready (RxRDYA) — This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR, if after this read there are no more characters still in the FIFO.

SRB — Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR — Output Port Configuration Register

OPCR[7] — OP7 Output Select — This bit programs the OP7 output to provide one of the following:

- The complement of OPR[7]
- The channel B transmitter interrupt output, which is the complement of TxRDYB. When in this mode OP7 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[6] — OP6 Output Select — This bit programs the OP6 output to provide one of the followng:

- The complement of OPR[6]
- The channel A transmitter interrupt output, which is the complement of TxRDYA. When in this mode OP6 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[5] — OP5 Output Select — This bit programs the OP5 output to provide one of the following:

- The complement of OPR[5]
- The channel B receiver interrupt output, which is the complement of ISR[5]. When in this mode OP5 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[4] — OP4 Output Select — This bit programs the OP4 output to provide one of the following:

- The complement of OPR[4]
- The channel A receiver interrupt output, which is the complement of ISR[1]. When in this mode OP4 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] — OP3 Output Select — This field programs the OP3 output to provide one of the following:

- The complement of OPR[3]
- The counter/timer output, in which case OP3 acts as an open collector output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains high until terminal count is reached, at which time it goes low. The output returns to the high state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- The 1X clock for the channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] — OP2 Output Select — This field programs the OP2 output to provide one of the following:

- The complement of OPR[2]
- The 16X clock for the channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- The 1X clock for the channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

Preliminary

ACR — Auxiliary Control Register

ACR[7] — Baud Rate Generator Set Select — This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05K, 1.2K, 2.4K, 4.8K, 7.2K, 9.6K, and 38.4K baud.

Set 2: 75, 110, 134.5, 150, 300, 600, 1.2K, 1.8K, 2.0K, 2.4K, 4.8K, 9.6K, and 19.2K baud.

The selected set of rates is available for use by the channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in table 3.

ACR[6:4]—Counter/Timer Mode and Clock Source Select — This field selects the operating mode of the counter/timer and its clock source as shown in table 4.

ACR[3:0] — IP3, IP2, IP1, IP0 Change of State Interrupt Enable — This field selects which bits of the Input Port Change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state, the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR — Input Port Change Register

IPCR[7:4] — IP3, IP2, IP1, IP0 Change of State — These bits are set when a change of state, as defined in the Input Port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register.

The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] — IP3, IP2, IP1, IP0 Current State — These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR — Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR — the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] — Input Port Change Status — This bit is a '1' when a change of state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] — Channel B Change in Break — This bit, when set, indicates that the channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a channel B 'reset break change interrupt' command.

ISR[5] — Channel B Receiver Ready or FIFO Full — The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the channel B FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

Table 3 BAUD RATE GENERATOR CHARACTERISTICS CRYSTAL OR CLOCK = 3.6864MHz

NOMINAL RATE (BAUD)	ACTUAL 16X CLOCK (KHz)	ERROR (PERCENT)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

NOTE:
Duty cycle of 16X clock is 50% ± 1%.

Table 4 ACR [6:4] FIELD DEFINITION

ACR[6:4]	MODE	CLOCK SOURCE
0 0 0	Counter	External (IP2)[1]
0 0 1	Counter	TXCA — 1X clock of channel A transmitter
0 1 0	Counter	TXCB — 1X clock of channel B transmitter
0 1 1	Counter	Crystal or external clock (X1/CLK) divided by 16
1 0 0	Timer	External (IP2)[1]
1 0 1	Timer	External (IP2) divided by 16[1]
1 1 0	Timer	Crystal or external clock (X1/CLK)
1 1 1	Timer	Crystal or external clock (X1/CLK) divided by 16

[1]In these modes, the channel B receiver clock should normally be generated from the baud rate generator.

Preliminary

ISR[4] — Channel B Transmitter Ready — This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] — Counter Ready — In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] — Channel A Change in Break — This bit, when set, indicates that the channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a channel A 'reset break change interrupt' command.

ISR[1] — Channel A Receiver Ready or FIFO Full — The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the channel A FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[0] — Channel A Transmitter Ready — This bit is a duplicate of TxRDYA (SRA[2]).

IMR — Interrupt Mask Register

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3–OP7 or the reading of the ISR.

CTUR and CTLR — Counter/Timer Registers

The CTUR and CTLR hold the eight MSB's and eight LSB's respectively of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is 0002_{16}. Note that these registers are write-only and cannot be read by the CPU.

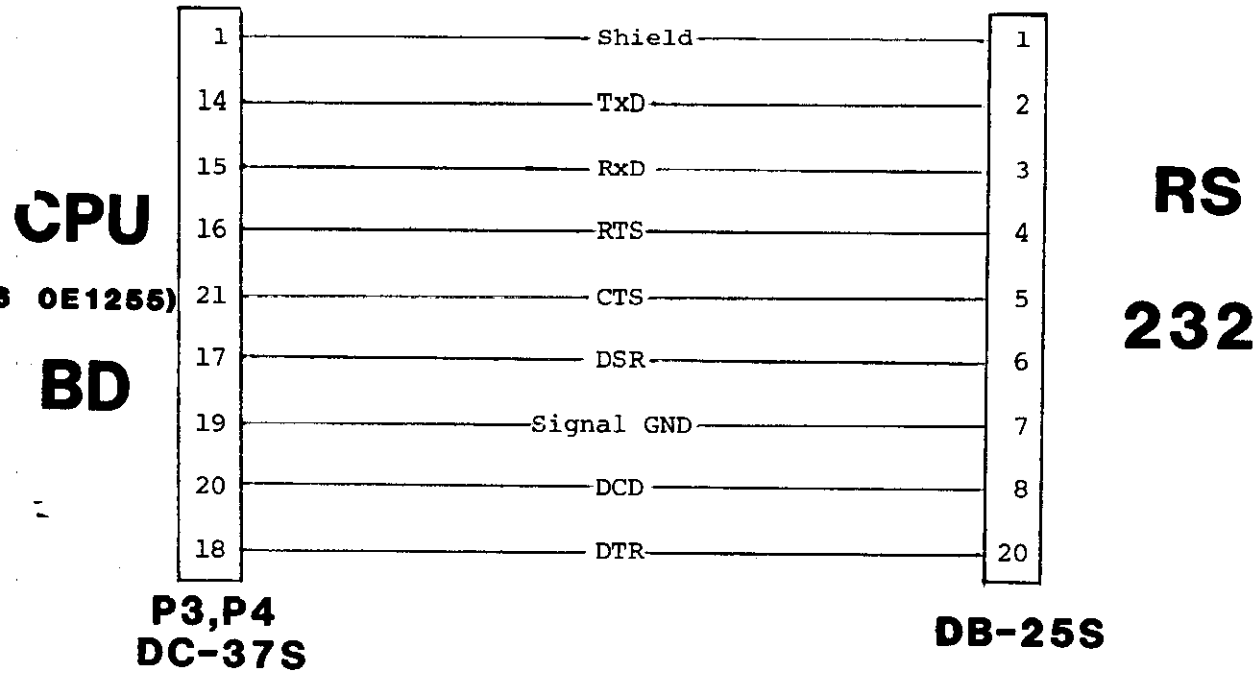
In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. In this mode the C/T runs continuously. Receipt of a start counter command (read with A3–A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR. The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3–A0 = 1111). The command, however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count (0000_{16}), the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains high until terminal count is reached, at which time it goes low. The output returns to the high state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

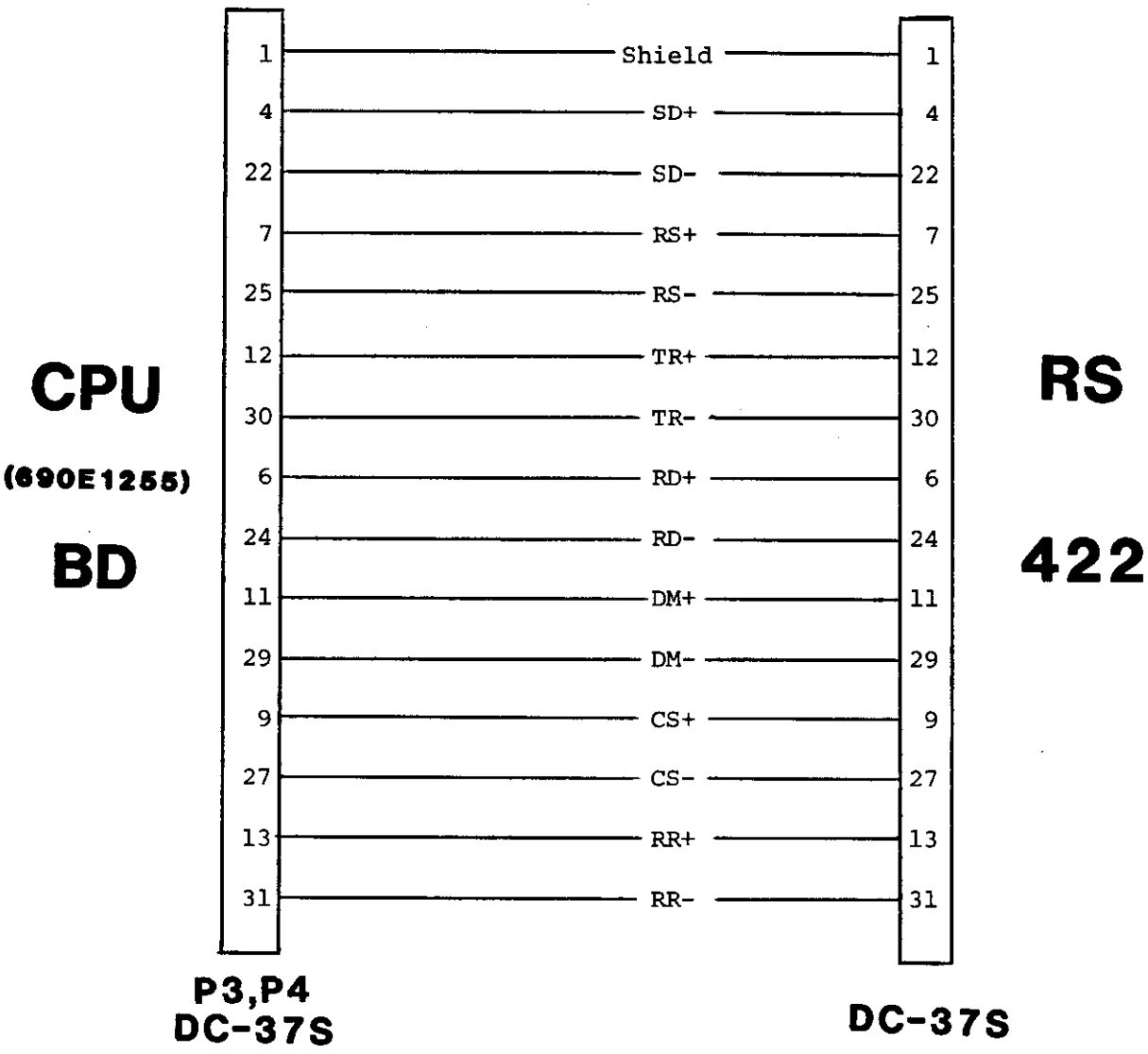
In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8-bits to the upper 8-bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

IVR — Interrupt Vector Register

This register contains the interrupt vector. The register is initialized to H'0F' by RESET. The contents of the register are placed on the data bus when the DUART responds to a valid interrupt acknowledge cycle.



CPU-RS232 PORT CABLE DIAGRAM



CPU-RS422 PORT CABLE DIAGRAM

CPU PALS

NAME	DEVICE	COMMENTS
CPU BOARD		
CPU-01AA-M60	12L6	MAP DECODER
CPU-02AA-M33	12L6	EPROM & RAM DECODER (27128)
CPU-03AA-M34	12L6	EPROM DECODER (27128)
CPU-04AA-M30	14L4	PERIPHERAL DECODER
CPU-04AB-M30	14L4	PAL FOR 8K EEPROM---option
CPU-05AA-M35	14L4	DTACK GENERATOR
CPU-06AA-M54	12L6	INTERRUPT HANDLER

HITACHI IC MEMORIES

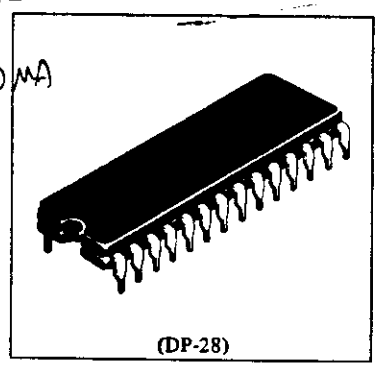
HM6264LP-10, HM6264LP-12, HM6264LP-15

HITACHI

8192-word x 8-bit High Speed Static CMOS RAM

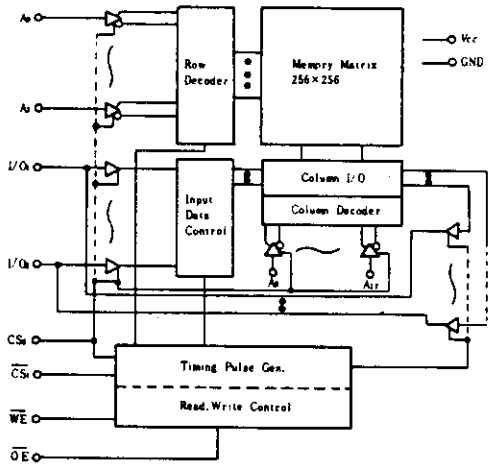
■ FEATURES

- Fast access Time — 100ns/120ns/150ns (max.)
- Low Power Standby — Standby: 0.01mW (typ.)
  Low Power Operation — Operating: 200mW (typ.)
- Capability of Battery Back-up Operation
- Single +5V Supply
- Completely Static Memory. . . . . No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

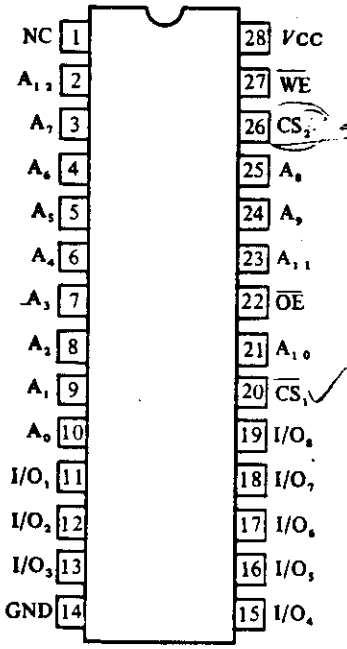


(DP-28)

■ BLOCK DIAGRAM



■ PIN APPRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns: −3.0V

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.3*	–	0.8	V

* Pulse Width 50ns: −3.0V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{in}=GND to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, $I_{I/O}$=0mA	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $\overline{CS1}$=V_{IL}, CS2=V_{IH}	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}, $I_{I/O}$=0mA	–	1	3	mA
	I_{SB1}**	$\overline{CS1}$≧V_{CC}−0.2V, CS2≧V_{CC}−0.2V or CS2≦0.2V	–	2	100	μA
	I_{SB2}**	CS2≦0.2V	–	2	100	μA
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	–	–	V

* Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
** V_{IL} min=−0.3V

■ CAPACITANCE (f= 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10ns
Input and Output Timing Reference Level: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

• READ CYCLE

Item		Symbol	HM6264LP-10		HM6264LP-12		HM6264LP-15		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	100	–	120	–	150	–	ns
Address Access Time		t_{AA}	–	100	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	100	–	120	–	150	ns
	CS2	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	50	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	10	–	15	–	ns

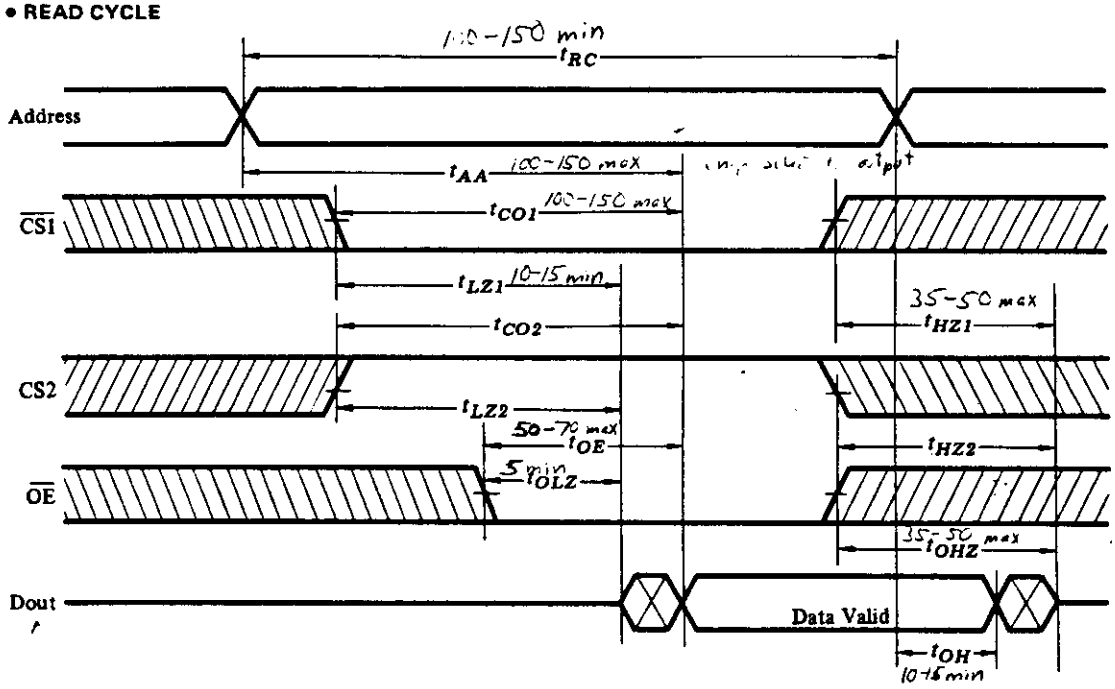
NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• **WRITE CYCLE**

Item		Symbol	HM6264LP-10		HM6264LP-12		HM6264LP-15		Unit
			min	max	min	max	min	max	
Write Cycle Time		t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write		t_{CW}	80	–	85	–	100	–	ns
Address Setup Time		t_{AS}	0	–	0	–	0	–	ns
Address Valid to End of Write		t_{AW}	80	–	85	–	100	–	ns
Write Pulse Width		t_{WP}	60	–	70	–	90	–	ns
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	t_{WR1}	5	–	5	–	10	–	ns
	CS2	t_{WR2}	15	–	15	–	15	–	ns
Write to Output in High Z		t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap		t_{DW}	40	–	50	–	60	–	ns
Data Hold from Write Time		t_{DH}	0	–	0	–	0	–	ns
$\overline{OE}$ to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write		t_{OW}	5	–	5	–	10	–	ns

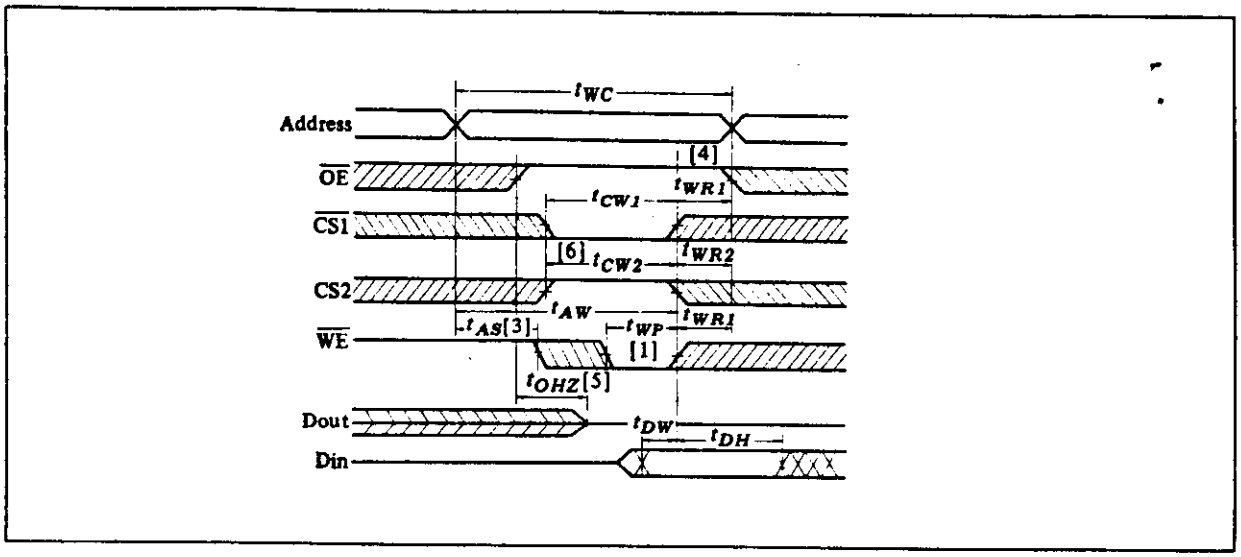
■ TIMING WAVEFORM

• **READ CYCLE**

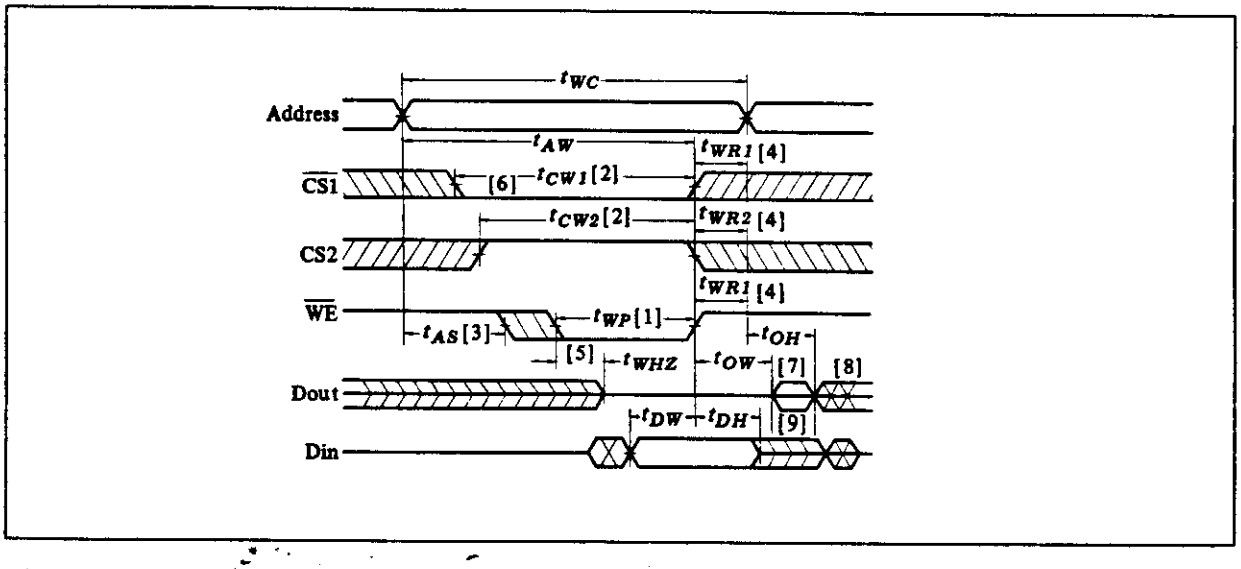


NOTES: 1) $\overline{WE}$ is high for Read Cycle
2) When $\overline{CS1}$ is Low and CS2 is High the address input must not be in the high impedance state.

• **WRITE CYCLE (1) ($\overline{OE}$ clock)**



• **WRITE CYCLE (2) ($\overline{OE}$ Low Fix)**



NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transtion among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginninng of write to the end of write.

2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

3) t_{AS} is measured from the address valid to the beginning of write.

4) t_{WR} is measured from the end of write to the address change.
t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high.
t_{WR2} applies in case a write ends at CS2 going low.

5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

7) Dout is in the same phase of written data of this cycle.

8) Dout is the read data of the new address.

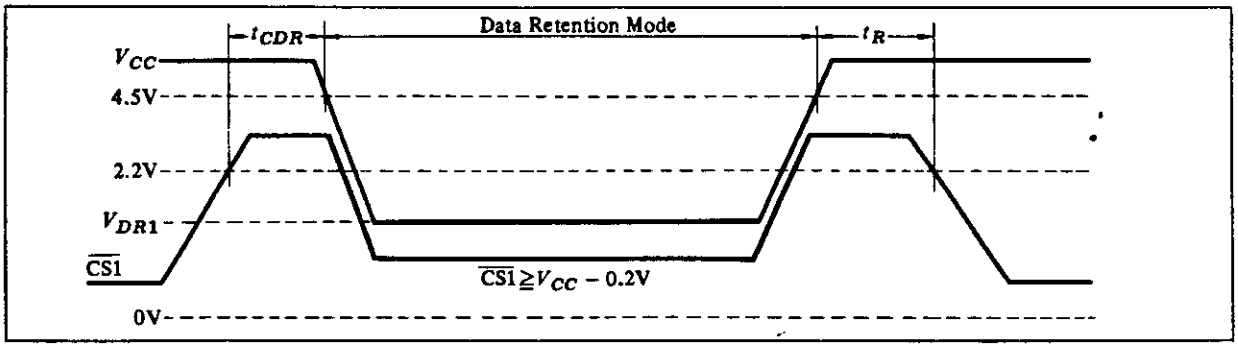
9) If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70 °C)

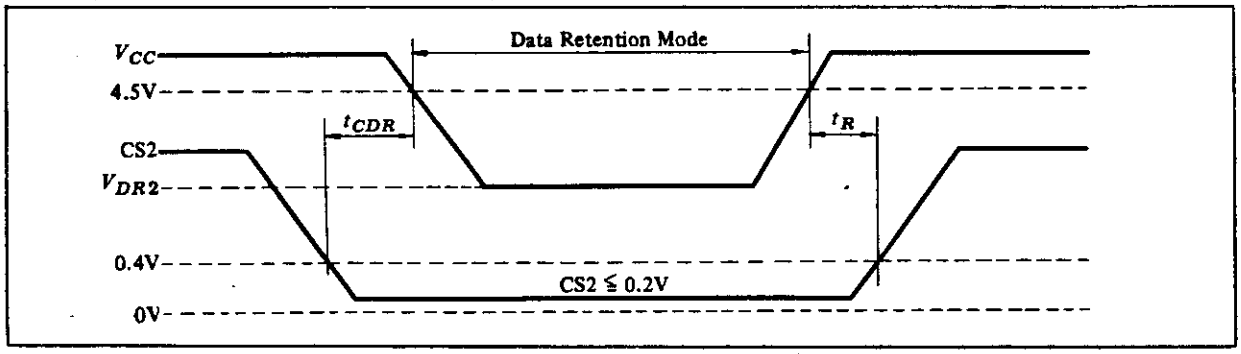
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geqq V_{CC} - 0.2V$, $CS2 \geqq V_{CC} - 0.2V$ or $CS2 \leqq 0.2V$	2.0	–	–	V
	V_{DR2}	$CS2 \leqq 0.2V$	2.0	–	–	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3.0V, $\overline{CS1} \geqq V_{CC} - 0.2V$, $CS2 \geqq V_{CC} - 0.2V$ or $CS2 \leqq 0.2V$	–	1	50*	μA
	I_{CCDR2}	V_{CC} = 3.0V, $CS2 \leqq 0.2V$	–	1	50*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}**	–	–	ns

* V_{IL} min = –0.3V
** t_{RC} = Read Cycle Time

• LOW Vcc DATA RETENTION WAVEFORM (2) ($\overline{CS1}$ Controlled)



• LOW Vcc DATA RETENTION WAVEFORM (2) (CS2 Controlled)



NOTE: CS_2 controls Address buffer, $\overline{WE}$ buffer, $\overline{CS_1}$ buffer and Din buffer. If CS_2 controls data retention mode, Vin level (Address, $\overline{WE}$, $\overline{CS_1}$, I/O) can be in the high impedance state. If $\overline{CS_1}$ controls data retention mode, CS_2 must be $CS_2 \geqq$ Vcc–0.2V or $CS_2 \leqq 0.2V$. The other inputs level (address, $\overline{WE}$, I/O) can be in the high impedance state.

PRELIMINARY DATA SHEET
Characteristics Subject to Change
Without Notice.

X2816A 2K x 8 Bit Electrically Erasable PROM
X2804A 512 x 8 Bit Electrically Erasable PROM

5 Volt Programmable E²PROMs

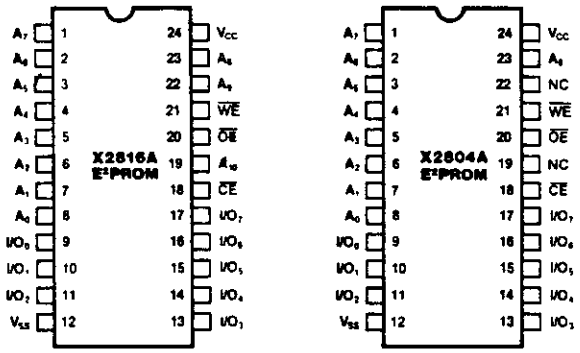
- **Simple Byte Write Operation**
  - **No High Voltages Necessary**
  - **Single TTL level $\overline{WE}$ Signal Modifies Data**
  - **Internally Latched Addresses and Data**
  - **Automatic Write Time-out**
  - **Noise Protected $\overline{WE}$ Pin**
- **Conforms to JEDEC Byte-wide Standard**
- **Reliable N-Channel Floating Gate MOS Technology**
- **Single 5-Volt Supply**
- **Byte Write Time: 10ms Max.**
- **Fast Access Time: 300ns Max.**
- **Low Power Dissipation**
  - **Active Current X2816A: 110mA Max.**
    X2804A: 80mA Max.
  - **Standby Current: 50mA Max.**

The Xicor X2816A (16,384 bits) and X2804A (4,096 bits) are electrically erasable programmable read-only memories (E²PROMs) with unprecedented ease-of-use features. Xicor E²PROM data can be modified using simple TTL level signals and a *single 5-volt power supply.* In addition, Xicor E²PROMs are operationally and pin compatible with existing 2K x 8 byte-programmable E²PROMs which require an additional high voltage power supply for programming. (See *optional* high voltage programming compatible mode.) Writing data in Xicor E²PROMs is analogous to writing data in a static RAM. A 200ns TTL low level signal to the $\overline{WE}$ pin initiates a byte write operation which is automatically timed out in a maximum of 10ms. Since addresses and data are internally latched, Xicor E²PROMs free the system for other tasks during the 10ms period, such as programming other Xicor E²PROMs. In addition to byte modification capability, a 10ms total chip erase feature is provided.

Xicor E²PROMs use a 2-line control architecture, $\overline{CE}$ and $\overline{OE}$, to eliminate bus contention in a system environment. A power down mode is featured. In the standby mode, power consumption is reduced by 64% without increasing access time. The standby mode is achieved by applying a $\overline{CE}$ high signal.

The X2816A and X2804A are fabricated with the same reliable n-channel floating gate MOS technology used in Xicor's popular 5-Volt programmable NOVRAM memories.

PIN CONFIGURATIONS 24 PIN DIP.600"



PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
I/O_0-I/O_7	DATA INPUTS/OUTPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
V_{CC}	+5V
V_{SS}	GROUND
NC	NO CONNECT

MODE SELECTION

Standard Xicor 5V-Programmable Mode

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
H	X	X	Standby	High Z	Standby
L	L	H	Read	D_{OUT}	Active
L	H	L	Byte Write	D_{IN}	Active
L	H	H	Read and Write Inhibit	High Z	Active

Preliminary Information Sheet
December 1982 Stock No. 200-012

XICOR, Inc., 851 Buckeye Court, Milpitas, California 95035 (408) 946-6920 TWX 910-379-0033

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	−10°C to +85°C
Storage Temperature	−65°C to +125°C
Voltage on any Pin with Respect to Ground	−1.0V to +6V
D.C. Output Current	5mA
$\overline{OE}$ and $\overline{WE}$ Pins During *Optional* High Voltage Mode	24.0V

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Limits: X2816A			Limits: X2804A			Units	Test Conditions
		Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.		
I_{CC}	V_{CC} Current (Active)			110			80	mA	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = OPEN Other Inputs = 5.5 V
I_{SB}	V_{CC} Current (Standby)			50			50	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = OPEN Other Inputs = 5.5 V
I_{LI}	Input Leakage Current			10			10	μA	$V_{IN} = 5.5$ V
I_{LO}	Output Leakage Current			10			10	μA	$V_{OUT} = 5.5$ V
V_{IL}	Input Low Voltage	−1.0		0.8	−1.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6	2.0		6	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	$I_{OL} = 2.1$mA
V_{OH}	Output High Voltage	2.4			2.4			V	$I_{OH} = -400\mu A$

CAPACITANCE[2]

$T_A = 25°C$, $f = 1.0$ MHz, $V_{CC} = 5V$

Symbol	Test	Max.	Unit	Conditions
$C_{I/O}$	Input/Output Capacitance	10	pF	$V_{I/O} = 0$ V
C_{IN}	Input Capacitance	6	pF	$V_{IN} = 0$ V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0 to 3.0 Volts
Input Rise and Fall Times	10 nsec
Input and Output Timing Levels	1.5 Volts
Output Load	1 TTL Gate and $C_L = 100$ pF

AC CHARACTERISTICS

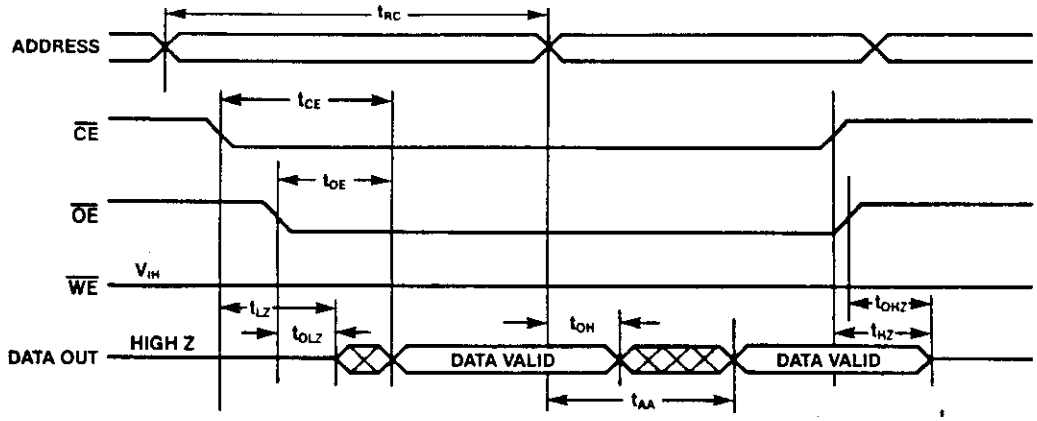
$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Read Cycle

Standard Xicor 5V-Programmable Mode

Symbol	Parameter	X2816A/ X2804A Limits		X2816A-35/ X2804A-35 Limits		X2816A-45/ X2804A-45 Limits	
		Min.	Max.	Min.	Max.	Min.	Max.
t_{RC}	Read Cycle Time	300		350		450	
t_{CE}	Chip Enable Access Time		300		350		450
t_{AA}	Address Access Time		300		350		450
t_{OE}	Output Enable Access Time		120		135		150
t_{LZ}	Chip Enable to Output in Low Z	10		10		10	
t_{HZ}	Chip Disable to Output in High Z	10	100	10	100	10	100
t_{OLZ}	Output Enable to Output in Low Z	50		50		50	
t_{OHZ}	Output Disable to Output in High Z	10		10		10	
t_{OH}	Output Hold from Address Change	20		20		20	

Read Cycle



Write Cycle

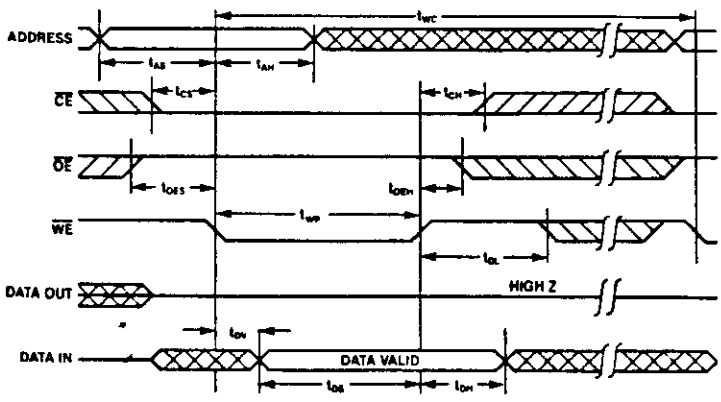
Standard Xicor 5V-Programmable Mode

Symbol	Parameter	Limits			Units
		Min.	Typ.[1]	Max.	
t_{WC}	Write Cycle Time	10			ms
t_{AS}	Address Set-Up Time	10			ns
t_{AH}	Address Hold Time	120			ns
t_{CS}	Write Set-Up Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	Chip Enable to End of Write Input	150			ns
t_{OES}	Output Enable Set-Up Time	10			ns
t_{OEH}	Output Enable Hold Time	10			ns
t_{WP}[3]	Write Pulse Width	150			ns
t_{DL}	Data Latch Time	50			ns
t_{DV}[4]	Data Valid Time			1	µs
t_{DS}	Data Set-Up Time	50			ns
t_{DH}	Data Hold Time	10			ns

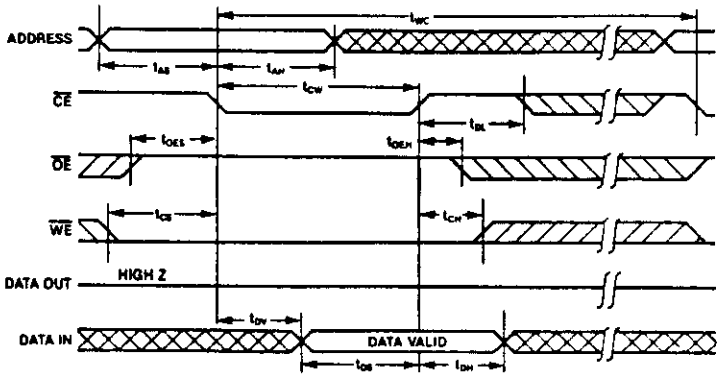
Endurance

Xicor E²PROMs are designed to perform up to 10,000 write cycles per byte.

$\overline{WE}$ Controlled Write Cycle



$\overline{CE}$ Controlled Write Cycle



OPTIONAL HIGH VOLTAGE MODES

Xicor's E^2PROMs require only 5 Volts for writing. As a user option, the X2816A and X2804A were also designed to be operationally and pin compatible with high voltage erasable and programmable E^2PROMs. This page describes the *optional* high voltage modes.

MODE SELECTION

Optional High Voltage Programmable Compatible Mode

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
L	H	12V-22V	Byte Erase	D_{IN} = H	Active
L	H	12V-22V	Byte Write	D_{IN}	Active
L	12V-22V	12V-22V	Chip Erase	D_{IN} = H	Active

DC OPERATING CHARACTERISTICS

$T_A = 0°$ to 70°C, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

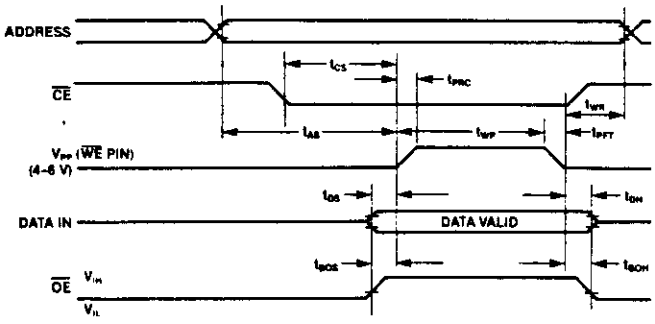
Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.[1]	Max.		
V_{PP}[5]	Write/Erase Voltage	12		22	V	
$I_{PP(W)}$	V_{PP} Current (Byte Erase/Write)			0.01	mA	$\overline{CE} = V_{IL}$
V_{OE}	$\overline{OE}$ Voltage (Chip Erase)	12		22	V	I_{OE} = 10 µA
$I_{PP(I)}$	V_{PP} Current Inhibit			0.01	mA	$V_{PP} = 22V$, $\overline{CE} = V_{IH}$
$I_{PP(C)}$	V_{PP} Current (Chip Erase)			0.01	mA	

AC CHARACTERISTICS

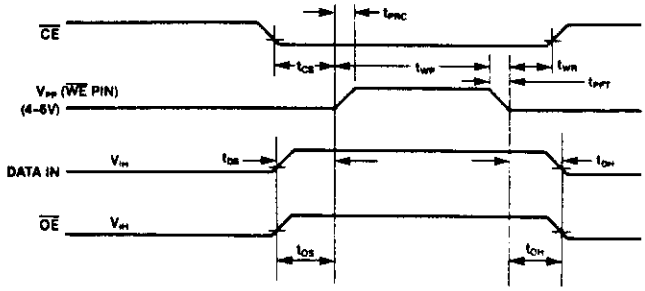
$T_A = 0°$ to 70°C, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.[1]	Max.		
t_{AS}	Add to V_{PP} Set-Up Time	10			ns	
t_{CS}	$\overline{CE}$ to V_{PP} Set-Up Time	10			ns	
t_{DS}	Data to V_{PP} Set-Up Time	0			ns	
t_{DH}	Data Hold Time	50			ns	$V_{PP} = 6V$
t_{WP}	Write Pulse Width	150ns		15ms		
t_{WR}	Write Recovery Time	50			ns	$V_{PP} = 6V$
t_{OS}	Chip Erase Set-Up Time	10			ns	$V_{PP} = 6V$, $V_{OE} = 12V$
t_{OH}	Chip Erase Hold Time	10			ns	$V_{PP} = 6V$, $V_{OE} = 12V$
t_{PRC}	V_{PP} RC Time Constant			750	µs	
t_{PFT}	V_{PP} Fall Time			100	µs	$V_{PP} = 6V$
t_{BOS}	Byte Erase/Write Set-Up Time	10			ns	$V_{PP} = 6V$
t_{BOH}	Byte Erase/Write Hold Time	10			ns	$V_{PP} = 6V$

Byte Erase or Byte Write Cycle



Chip Erase Cycle



X2816A and X2804A DEVICE OPERATION

ADDRESSES (A_0-A_{10}):
E^2PROM bytes are selected for reading or writing by the address pins.

CHIP-ENABLE ($\overline{CE}$):
A device is selected when $\overline{CE}$ is LOW. A power down mode is achieved when $\overline{CE}$ is HIGH. In this standby mode power consumption is reduced by approximately 64%.

DATA-IN/DATA-OUT (I/O_0-I/O_7):
Data is written into or read from a selected device through the I/O pins. The I/O pins are in the high impedance state when $\overline{CE}$ is HIGH, when a write operation is in progress, or when $\overline{OE}$ is HIGH.

OUTPUT-ENABLE ($\overline{OE}$):
Reading data from Xicor E^2PROMs is analogous to reading data from a static RAM. Data is read from a selected device with $\overline{WE}$ HIGH and $\overline{OE}$ LOW.
Xicor E^2PROMs use a 2-line control architecture to eliminate bus contention in a system environment. The I/O pins are in a high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is HIGH.

WRITE ENABLE ($\overline{WE}$):
Standard 5V-Programmable Mode
Writing data in Xicor E^2PROMs is analogous to writing data into a static RAM. A $\overline{WE}$ LOW applied to a selected device with $\overline{OE}$ HIGH initiates a cycle that writes data at the I/O pins into a location selected by the address pins. A byte write cycle, once initiated, will automatically continue to completion in less than 10ms. During a byte write cycle, addresses are latched on the last falling edge of $\overline{CE}$ or $\overline{WE}$; data is latched on the first rising edge of $\overline{CE}$ or $\overline{WE}$. System design is greatly simplified since writing requires only a single 5V supply and a single TTL level $\overline{WE}$ signal. Addresses and data are conveniently latched in less than 200ns during a byte write.

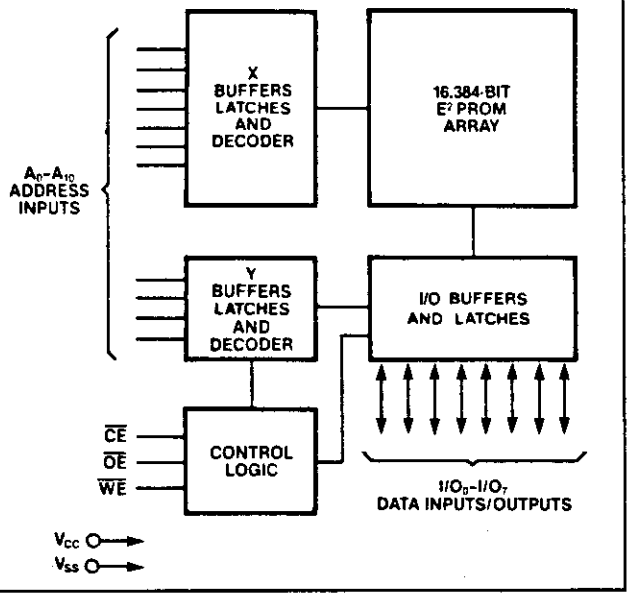
***Optional* High Voltage Programming Compatible Mode**
Although Xicor's E^2PROMs require only 5 Volts for programming, they were designed to be operationally and pin compatible with 2K x 8 byte erasable programmable E^2PROMs requiring additional high voltage programming supplies. These other high voltage E^2PROMs generally require two separate high voltage operations to reprogram a byte of information; the first to erase the previous information and the second to program the new information. As in the previously discussed 5 Volt programmable mode, it is unnecessary to use these two separate steps to write a byte of information into Xicor E^2PROMs. It is only necessary for the user to write the new data "over" the old data at each byte location. To further assist the user, Xicor E^2PROMs will accept the two step approach of high voltage E^2PROMs.

OPTIONAL HIGH VOLTAGE CHIP ERASE CYCLE
All data can be changed to "1" or erase state in one 10ms cycle by raising $\overline{OE}$ to 12-22V and bringing $\overline{WE}$ to 12-22V with all data inputs HIGH.

ENDURANCE
Xicor E^2PROMs are designed for applications requiring up to 10,000 write cycles per byte.

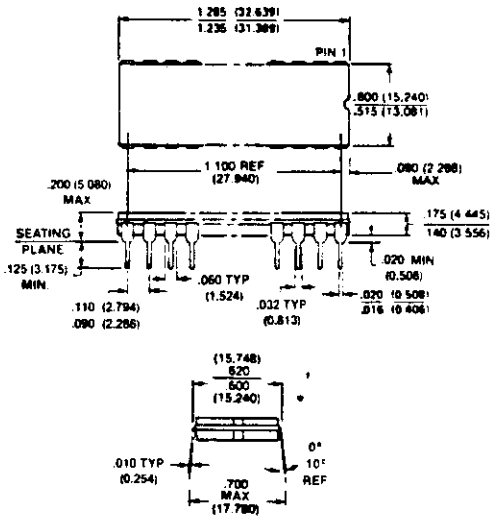
Notes:
(1) Typical values are for $T_A = 25°C$ and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.
(3) $\overline{WE}$ is noise protected. Less than a 20ns write pulse will not activate a write cycle.
(4) Data must be valid within 1μs maximum after the initiation of a write cycle.
(5) In *optional* high voltage programming mode $\overline{WE}$ is designated as V_{PP}.

FUNCTIONAL DIAGRAM X2816A (2K x 8)



PACKAGING INFORMATION

24-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



ORDERING INFORMATION

Part Number	Access Time (ns)	Memory Organization
X2816AD	300	2K x 8
X2816AD-35	350	2K x 8
X2816AD-45	450	2K x 8
X2804AD	300	512 x 8
X2804AD-35	350	512 x 8
X2804AD-45	450	512 x 8

Temperature Range Designations
X2816AD = 0°C to +70°C
X2816ADI = −40°C to +85°C
X2816ADM = −55°C to +125°C
X2804AD = 0°C to +70°C
X2804ADI = −40°C to +85°C
X2804ADM = −55°C to +125°C

INTERSIL

PRELIMINARY
Specifications Subject To Change Without Notice

ICL7665

Micropower Under-/ Over-Voltage Detector

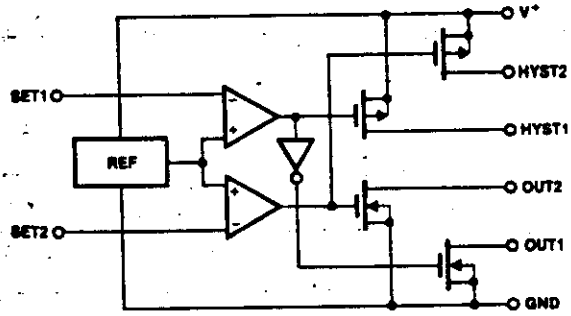
FEATURES

- Exceptionally low supply current (<3μA typ)
- Individually programmable upper and lower trip voltages and hysteresis levels
- Accurate on-chip bandgap reference, used by both detectors
- Up to 20mA output current sinking ability
- Wide supply voltage range

GENERAL DESCRIPTION

The ICL7665 contains two individually programmable voltage detectors on a single chip. Requiring only ~3μA for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and correction. Typical applications are battery-backup computer memories, battery-operated medical devices, radiation dosimeters, pocket pagers, portable calibrators and test instruments, and charging systems.

BLOCK DIAGRAM



Conditions*

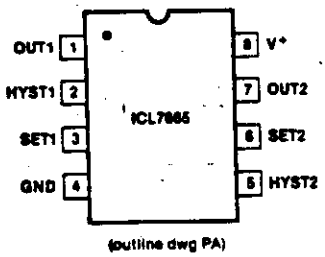
V_{SET1} > 1.3V, OUT1 switch ON — HYST1 switch ON
V_{SET1} < 1.3V, OUT1 switch OFF — HYST1 switch OFF
V_{SET2} > 1.3V, OUT2 switch OFF — HYST2 switch ON
V_{SET2} < 1.3V, OUT2 switch ON — HYST2 switch OFF

*See Operating Characteristics for exact thresholds.

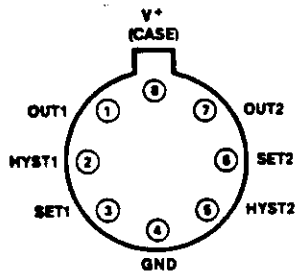
ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7665PA	– 20°C to + 70°C	8 Lead MiniDIP
ICL7665TV	– 20°C to + 70°C	8 Lead TO-99
ICL7665/D	—	DICE Only

PIN CONFIGURATIONS



(outline dwg PA)



(outline dwg TV)

5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... −0.3V to +18V
Output Voltages OUT1 and OUT2
(with respect to GND) (Note 2) ..... −0.3V to +18V
Output Voltages HYST1 and HYST2
(with respect to V^+) (Note 2) ..... +0.3V to −18V
Input Voltages SET1 and SET2
(Note 2) ..... (GND − 0.3V) to (V^+ + 0.3V)

Maximum Sink Output Current OUT1 and OUT2 ..... 25mA
Maximum Source Output Current
HYST1 and HYST2 ..... −25mA
Power Dissipation (Note 1) 200mW
Operating Temperature Range ..... −20°C to +70°C
Storage Temperature Range ..... −55°C to +125°C

Note 1: Derate above +25°C ambient temperature at 4mW/°C.

Note 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V^+ + 0.3V) or less than (GND − 0.3V) may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665 be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

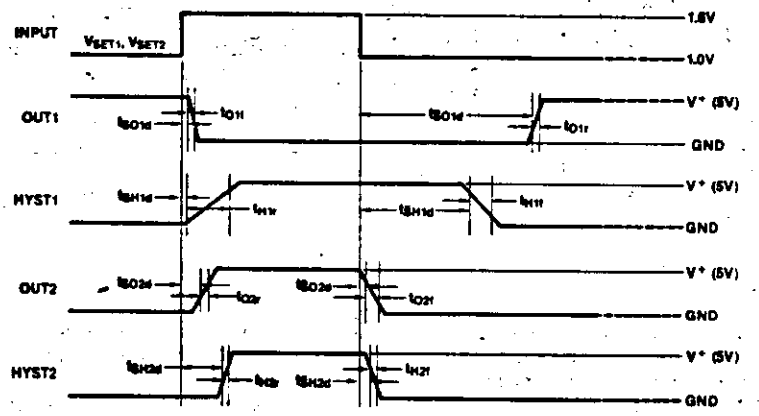
DC OPERATING CHARACTERISTICS (V^+ = 5V, T_A = +25°C, test circuit unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Supply Voltage	V^+	T_A = +25°C −20°C ≤ T_A ≤ +70°C	1.6 1.8		18.0 16.0	V
Supply Current	I^+	GND ≤ V_{SET1}, V_{SET2} ≤ V^+ All Outputs Open Circuit V^+ = 2V V^+ = 9V V^+ = 15V		 2.5 2.6 2.9	 10 10 15	µA
Input Trip Voltage	V_{SET1} V_{SET2}		1.15 1.2	1.3 1.3	1.45 1.4	V
Temperature Coefficient of V_{SET}	$\frac{\Delta V_{SET}}{\Delta T}$			200		ppm/°C
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{HYST2} = 1 MΩ		0.004		%/V
Output Leakage Currents on OUT and HYST	I_{OLK} I_{HLK}	V_{SET} = 0V or V_{SET} ≥ 2V		10 −10	200 −100	nA
	I_{OLK} I_{HLK}	V^+ = 15V, T_A = 70°C V^+ = 15V, T_A = 70°C			2000 −500	
Output Saturation Voltages	V_{OUT1} V_{OUT1} V_{OUT1}	V^+ = 2V, V_{SET1} = 2V, I_{OUT1} = 2mA V^+ = 5V, V_{SET1} = 2V, I_{OUT1} = 2mA V^+ = 15V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.2 0.1 0.06	0.5 0.3 0.2	
	V_{HYST1} V_{HYST1} V_{HYST1}	V^+ = 2V, V_{SET1} = 2V, I_{HYST1} = −0.5mA V^+ = 5V, V_{SET1} = 2V, I_{HYST1} = −0.5mA V^+ = 15V, V_{SET1} = 2V, I_{HYST1} = −0.5mA		−0.15 −0.05 −0.02	−0.3 −0.15 −0.10	
	V_{OUT2} V_{OUT2} V_{OUT2}	V^+ = 2V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 5V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 15V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.2 0.15 0.11	0.5 0.3 0.25	V
	V_{HYST2} V_{HYST2} V_{HYST2}	V^+ = 2V, V_{SET2} = 2V, I_{HYST2} = −0.2mA V^+ = 5V, V_{SET2} = 2V, I_{HYST2} = −0.5mA V^+ = 15V, V_{SET2} = 2V, I_{HYST2} = −0.5mA		−0.25 −0.43 −0.35	−0.8 −1.0 −0.8	
V_{SET} Input Leakage Current	I_{SET}	GND ≤ V_{SET} ≤ V^+		0.01	10	nA
ΔV_{SET} Input for Complete Output Change	ΔV_{SET}	R_{OUT} = 4.7kΩ, R_{HYST} = 20kΩ V_{OUT}LO = 1% V^+, V_{OUT}HI = 99% V^+		1		mV
Difference in Trip Voltages	$V_{SET1} - V_{SET2}$	R_{OUT}, R_{HYST} = 1MΩ		±5	±50	
Output/Hysteresis Difference		R_{OUT}, R_{HYST} = 1MΩ		±1		

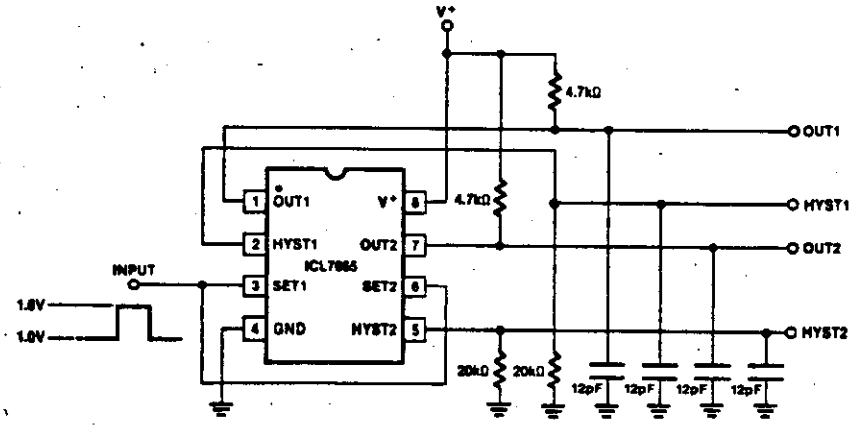
AC OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output Delay Times Input Going HI	t_{SO1d} t_{SH1d} t_{SO2d} t_{SH2d}	V_{SET} Switched from 1.0V to 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		70 80 120 230		µs
Input Going LO	t_{SO1d} t_{SH1d} t_{SO2d} t_{SH2d}	V_{SET} Switched from 1.6V to 1.0V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		1040 610 70 30		µs
Output Rise Times	t_{O1r} t_{O2r} t_{H1r} t_{H2r}	V_{SET} Switched between 1.0V and 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		120 80 330 25		µs
Output Fall Times	t_{O1f} t_{O2f} t_{H1f} t_{H2f}	V_{SET} Switched between 1.0V and 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		30 60 180 30		µs

SWITCHING WAVEFORMS

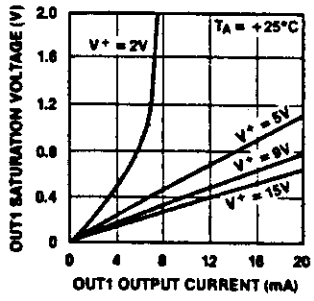


TEST CIRCUIT (Switching Response)

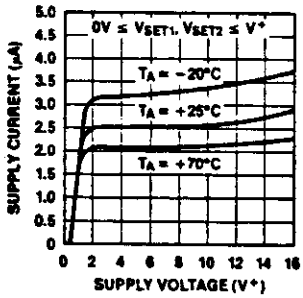


TYPICAL OPERATING CHARACTERISTICS

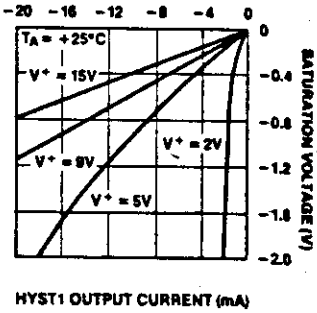
OUT1 Saturation Voltage as a Function of Output Current



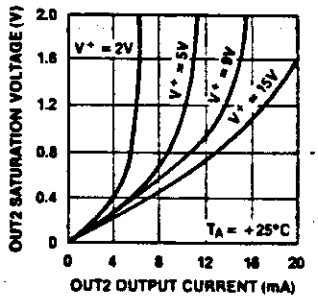
Supply Current as a Function of Supply Voltage



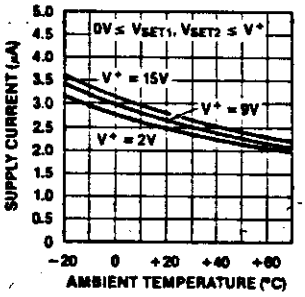
HYST1 Output Saturation Voltage vs HYST1 Output Current



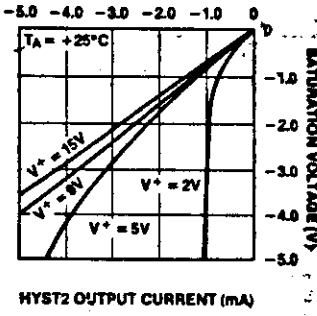
OUT2 Saturation Voltage as a Function of Output Current



Supply Current as a Function of Ambient Temperature



HYST2 Output Saturation Voltage vs HYST2 Output Current



5

DESCRIPTION

As shown in the Block Diagram, the ICL7665 consists of two comparators which compare input voltages on the SET1 and SET2 terminals to an internal 1.3V band-gap reference. The outputs from the two comparators drive open-drain N-channel transistors for OUT1 and OUT2, and open-drain P-channel transistors for HYST1 and HYST2 outputs. Each section, the Under-Voltage Detector and the Over-Voltage Detector, is independent of the other, although both use the internal 1.3V reference. The offset voltages of the two comparators will normally be unequal, so V_{SET1} will generally not quite equal V_{SET2}.

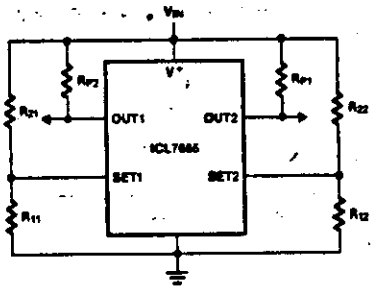
The input impedances of the SET1 and SET2 pins are extremely high, and for most practical applications can be ignored. The four outputs are open-drain MOS transistors, and when ON behave as low resistance switches to their respective supply rails. This minimizes errors in setting-up the hysteresis, and maximizes the output flexibility. The operating currents of the bandgap reference and the comparators are around 100nA each.

PRECAUTIONS

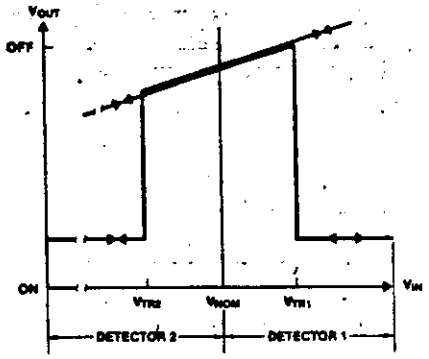
Junction-isolated CMOS devices like the ICL7665 have an inherent SCR or 4-layer PNPN structure distributed throughout the die. Under certain circumstances, this can be triggered into a potentially destructive high-current mode. This latch-up can be triggered by forward-biasing an input or output with respect to the power supply, or by applying excessive supply voltages. In very-low-current analog circuits, such as the ICL7665, this SCR can also be triggered by applying the input power supply extremely rapidly ("instantaneously"), e.g. through a low impedance battery and an ON/OFF switch with short lead lengths. The rate-of-rise of the supply voltage can exceed 100V/μs in such a circuit. A low-impedance capacitor (e.g. 0.05μF disc ceramic) between the V⁺ and GrouND pins of the ICL7665 can be used to reduce the rate-of-rise of the supply voltage in battery applications. In line-operated systems, the rate-of-rise of the supply is limited by other considerations, and is normally not a problem.

If the SET voltages must be applied before the supply voltage V⁺, the input current should be limited to less than 0.5mA by appropriate external resistors, usually required for voltage setting anyway. A similar precaution should be taken with the outputs if it is likely that they will be driven by other circuitry to levels outside the supplies at any time. See M011 for some other protection ideas.

APPLICATIONS



(a) Circuit Configuration



(b) Transfer Characteristics

Figure 1. Simple Threshold Detector

Figure 1 shows the simplest connection of the ICL7665 for threshold detection. From the graph (b), it can be seen that at low input voltages OUT1 is OFF, or high, while OUT2 is ON, or low. As the input rises (e.g. at power-on) toward V_{NOM} (usually the eventual operating voltage), OUT2 goes high on reaching V_{TR2}. If the voltage rises above V_{NOM} as much as V_{TR1}, OUT1 goes low. The equations giving V_{SET1} and V_{SET2} are, from Figure 1(a):

$$V_{SET1} = V_{IN} \frac{R_{11}}{(R_{11} + R_{21})} \qquad V_{SET2} = V_{IN} \frac{R_{12}}{(R_{12} + R_{22})}$$

Since the voltage to trip each comparator is nominally 1.3V, the value of V_{IN} for each trip point can be found from

$$V_{TR1} = V_{SET1} \frac{(R_{11} + R_{21})}{R_{11}} = 1.3 \frac{(R_{11} + R_{21})}{R_{11}} \text{ for detector 1 and}$$

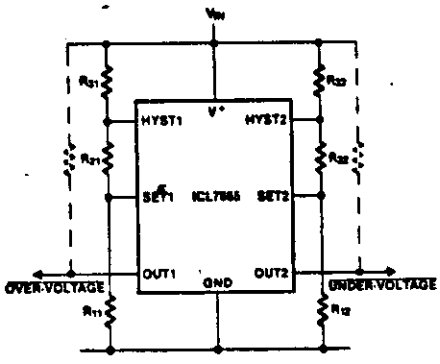
$$V_{TR2} = V_{SET2} \frac{(R_{12} + R_{22})}{R_{12}} = 1.3 \frac{(R_{12} + R_{22})}{R_{12}} \text{ for detector 2.}$$

Either detector may be used alone, as well as both together, in any of the circuits shown here.

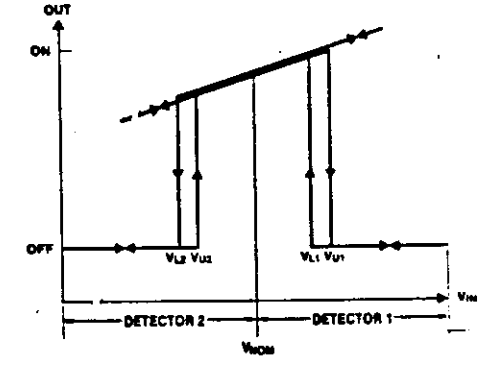
When V_{IN} is very close to one of the trip voltages, normal variations and noise may cause it to wander back and forth across this level, leading to erratic output ON and OFF conditions. The addition of hysteresis, making the trip points slightly different for rising and falling inputs, will avoid this condition.

Figure 2(a) shows how to set up such hysteresis, while Figure 2(b) shows how the hysteresis around each trip point produces switching action at different points depending on whether V_{IN} is rising or falling (the arrows indicate direction of change). The HYST outputs are basically switches which short out R_{31} or R_{32} when V_{IN} is above the respective trip point. Thus if the input voltage rises from a low value, the trip point will be controlled by R_{1n}, R_{2n} and R_{3n}, until the trip point is reached. As this value is passed, the detector changes state, R_{3n} is shorted out, and the trip point becomes controlled by only R_{1n} and R_{2n}, a lower value. The input will then have to fall to this new point to restore the initial comparator state, but as soon as this occurs, the trip point will be raised again.

An alternative circuit for obtaining hysteresis is shown in Figure 3. In this configuration, the HYST pins put the extra resistor in parallel with the upper setting resistor. The values of the resistors differ, but the action is essentially the same. The governing equations are given in Table 1. These ignore the effects of the resistance of the HYST outputs, but these can normally be neglected if the resistor values are above about 100kΩ.



(a) Circuit Configuration



(b) Transfer Characteristics

Figure 2. Threshold Detector with Hysteresis

APPLICATIONS (Continued)

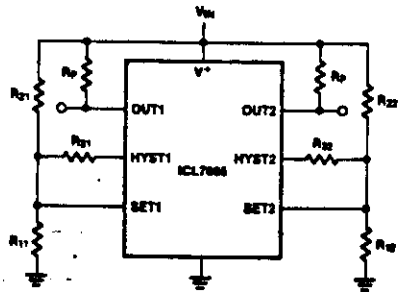


Figure 3. An Alternative Hysteresis Circuit

Table 1. Set-Point Equations

a) NO HYSTERESIS

Over-Voltage $V_{TRIP} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$

Under-Voltage $V_{TRIP} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$

b) HYSTERESIS PER FIGURE 2A

Over-Voltage V_{TRIP}

$$V_{U1} = \frac{R_{11} + R_{21} + R_{31}}{R_{11}} \times V_{SET1}$$

$$V_{L1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$$

Under-Voltage V_{TRIP}

$$V_{U2} = \frac{R_{12} + R_{22} + R_{32}}{R_{12}} \times V_{SET2}$$

$$V_{L2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$$

c) HYSTERESIS PER FIGURE 3

Over-Voltage V_{TRIP}

$$V_{U1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$$

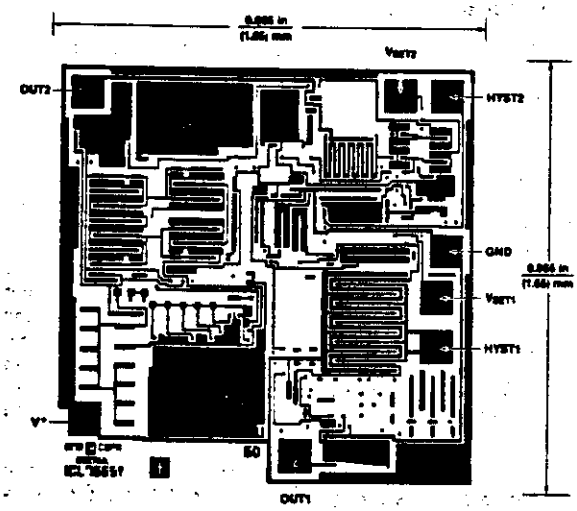
$$V_{L1} = \frac{R_{11} + \frac{R_{21}\,R_{31}}{R_{21} + R_{31}}}{R_{11}} \times V_{SET1}$$

Under-Voltage V_{TRIP}

$$V_{U2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$$

$$V_{L1} = \frac{R_{12} + \frac{R_{22}\,R_{32}}{R_{22} + R_{32}}}{R_{12}} \times V_{SET2}$$

CHIP TOPOGRAPHY

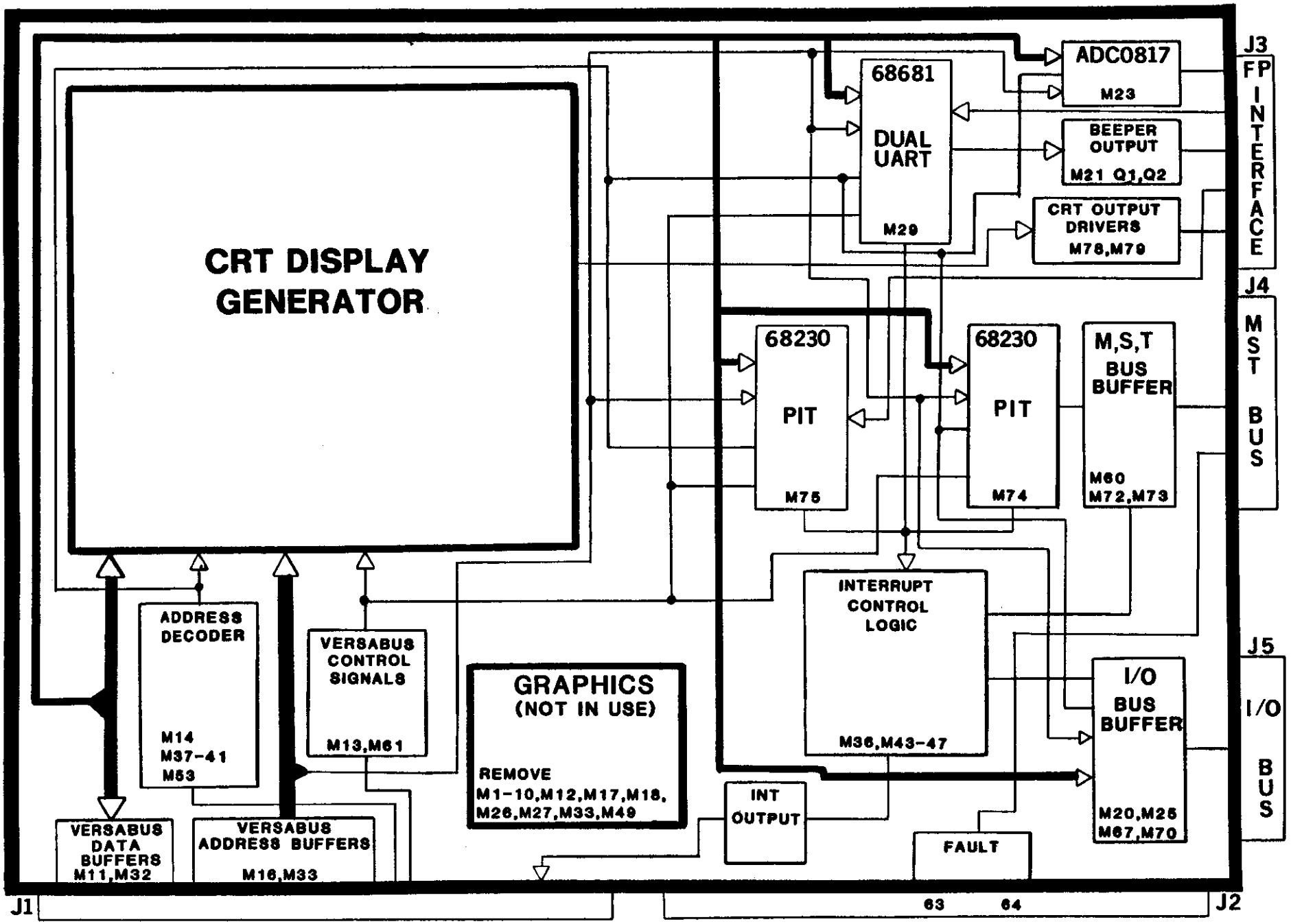


ICL7665

CRT BOARD

(690D1256)

BLOCK DIAGRAM- CRT BOARD



National Semiconductor

Analog-to-Digital Converters

ADC0816, ADC0817 8-Bit μP Compatible A/D Converters with 16-Channel Multiplexer

General Description

The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

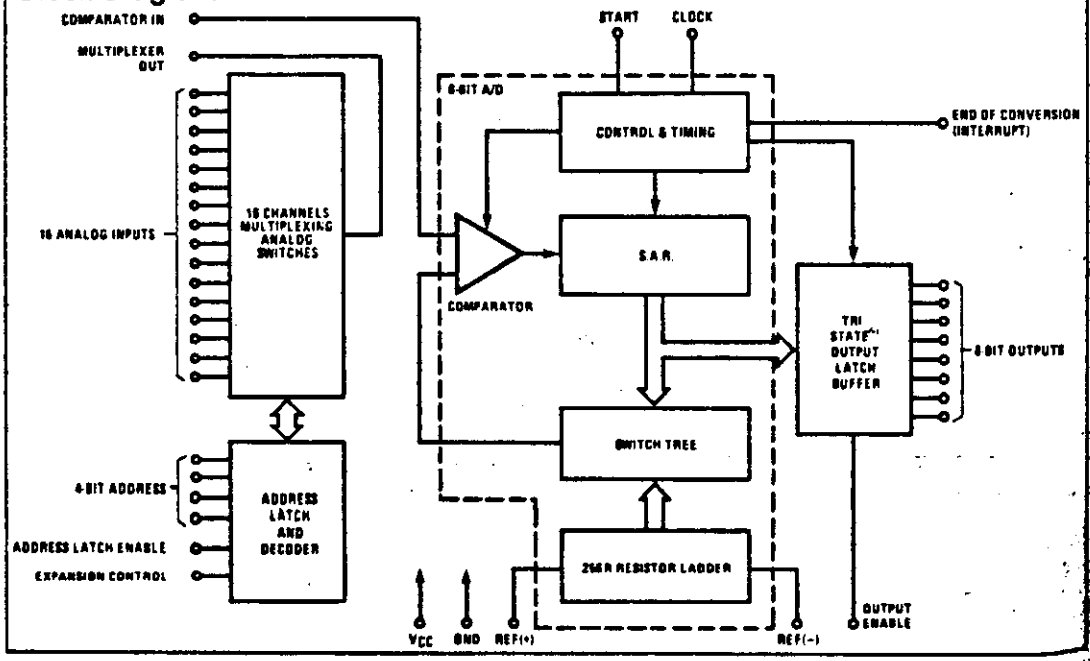
The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For similar performance in an 8-channel, 28-pin, 8-bit A/D converter, see the ADC0808, ADC0809 data sheet.

Features

- Resolution — 8-bits
- Total unadjusted error — ± 1/2 LSB and ± 1 LSB
- No missing codes
- Conversion time — 100 μs
- Single supply — 5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 16-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T^2L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 40-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Low power consumption — 15 mW
- Latched TRI-STATE® output
- Direct access to "comparator in" and "multiplexer out" for signal conditioning

Block Diagram



Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	−0.3V to 15V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0816CJ	−55°C ≤ T_A ≤ +125°C
ADC0816CCJ, ADC0816CCN, ADC0817CCN	−40°C ≤ T_A ≤ +85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}
Voltage at Any Pin Except Control Inputs	0V to V_{CC}
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	0V to 15V

Electrical Characteristics

Converter Specifications: V_{CC} = 5 V_{DC} = $V_{REF(+)}$, $V_{REF(-)}$ = GND, V_{IN} = $V_{COMPARATOR\ IN}$, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise stated.

Parameter		Conditions	Min	Typ	Max	Units
	ADC0816					
	Total Unadjusted Error (Note 5)	25°C			± 1/2	LSB
		T_{MIN} to T_{MAX}			± 3/4	LSB
	ADC0817					
	Total Unadjusted Error (Note 5)	0°C to 70°C			± 1	LSB
		T_{MIN} to T_{MAX}			± 1 1/4	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	4.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2−0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
	Comparator Input Current	f_c = 640 kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0816CJ 4.5V ≤ V_{CC} ≤ 5.5V, −55°C ≤ T_A ≤ +125°C unless otherwise noted. ADC0816CCJ, ADC0816CCN, ADC0817CCN 4.75V ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
R_{ON}	Analog Multiplexer ON Resistance	(Any Selected Channel)				
		T_A = 25°C, R_L = 10k		1.5	3	kΩ
		T_A = 85°C			6	kΩ
		T_A = 125°C			9	kΩ
ΔR_{ON}	Δ ON Resistance Between Any 2 Channels	(Any Selected Channel) R_L = 10k		75		Ω
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 5V,				
		T_A = 25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 0,				
		T_A = 25°C	−200			nA
		T_{MIN} to T_{MAX}	−1.0			μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN} = 15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN} = 0	−1.0			μA
I_{CC}	Supply Current	f_{CLK} = 640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0816CJ $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_A \le +125°C$ unless otherwise noted. ADC0816CCJ, ADC0816CCN, ADC0817CCN $4.75V \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$ unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\ \mu A$	$V_{CC}-0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6$ mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O = 1.2$ mA			0.45	V
I_{OUT}	TRI-STATE Output Current	$V_O = V_{CC}$			3	μA
		$V_O = 0$	-3			μA

Electrical Characteristics

Timing Specifications: $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $t_r = t_f = 20$ ns and $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)*		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S = 0\Omega$ *(Figure 5)*		1	2.5	μs
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L = 50$ pF, $R_L = 10$k *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	$C_L = 10$ pF, $R_L = 10$k *(Figure 8)*		125	250	ns
t_C	Conversion Time	$f_c = 640$ kHz, *(Figure 5)* (Note 7)	90	100	116	μs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		$8 + 2\ \mu s$	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs, (Note 7)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, and linearity errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Functional Description

Multiplexer: The device contains a 16-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address line and the expansion control line to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE				EXPANSION CONTROL
	D	C	B	A	
IN0	L	L	L	L	H
IN1	L	L	L	H	H
IN2	L	L	H	L	H
IN3	L	L	H	H	H
IN4	L	H	L	L	H
IN5	L	H	L	H	H
IN6	L	H	H	L	H
IN7	L	H	H	H	H
IN8	H	L	L	L	H
IN9	H	L	L	H	H
IN10	H	L	H	L	H
IN11	H	L	H	H	H
IN12	H	H	L	L	H
IN13	H	H	L	H	H
IN14	H	H	H	L	H
IN15	H	H	H	H	H
All Channels OFF	X	X	X	X	L

X = don't care

Additional single-ended analog signals can be multiplexed to the A/D converter by disabling all the multiplexer inputs using the expansion control. The additional external signals are connected to the comparator input and the device ground. Additional signal conditioning (i.e., prescaling, sample and hold, instrumentation amplification, etc.) may also be added between the analog input signal and the comparator input.

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached + 1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

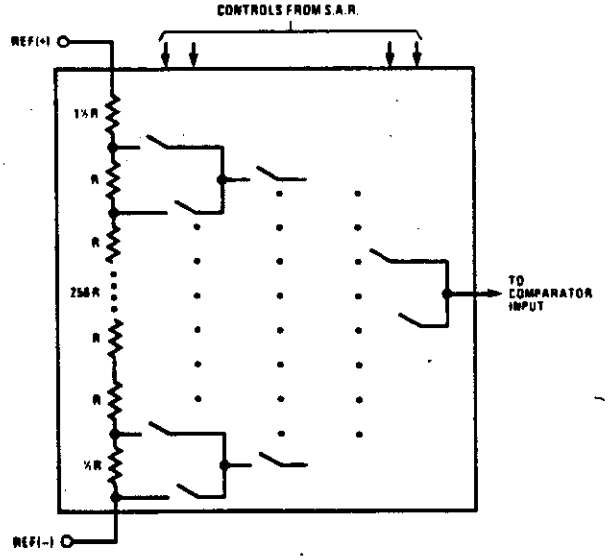


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0816, ADC0817, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0816 as measured using the procedures outlined in AN-179.

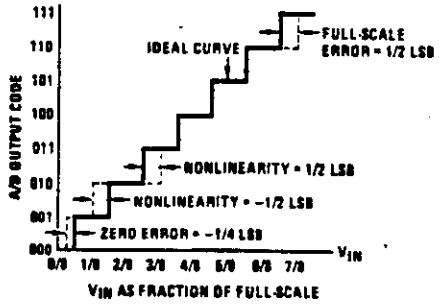


FIGURE 2. 3-Bit A/D Transfer Curve

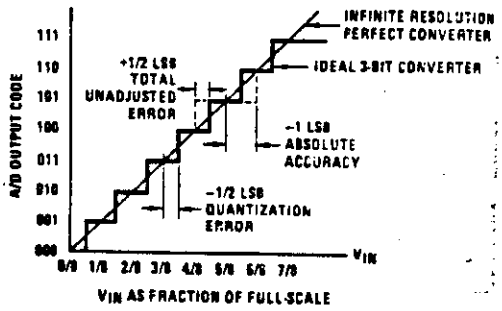


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

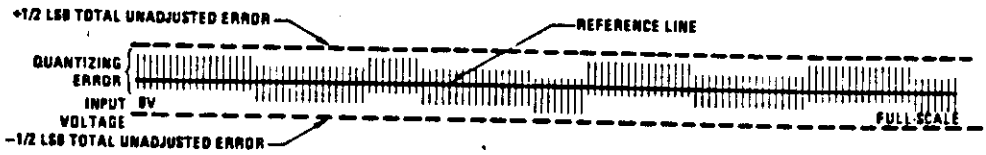
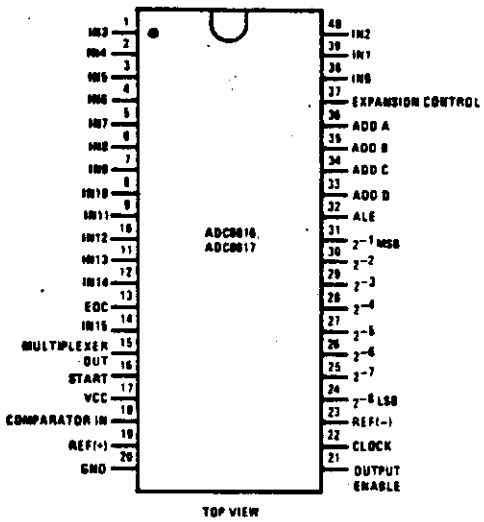


FIGURE 4. Typical Error Curve

Connection Diagram

Dual-In-Line Package



TOP VIEW

Timing Diagram

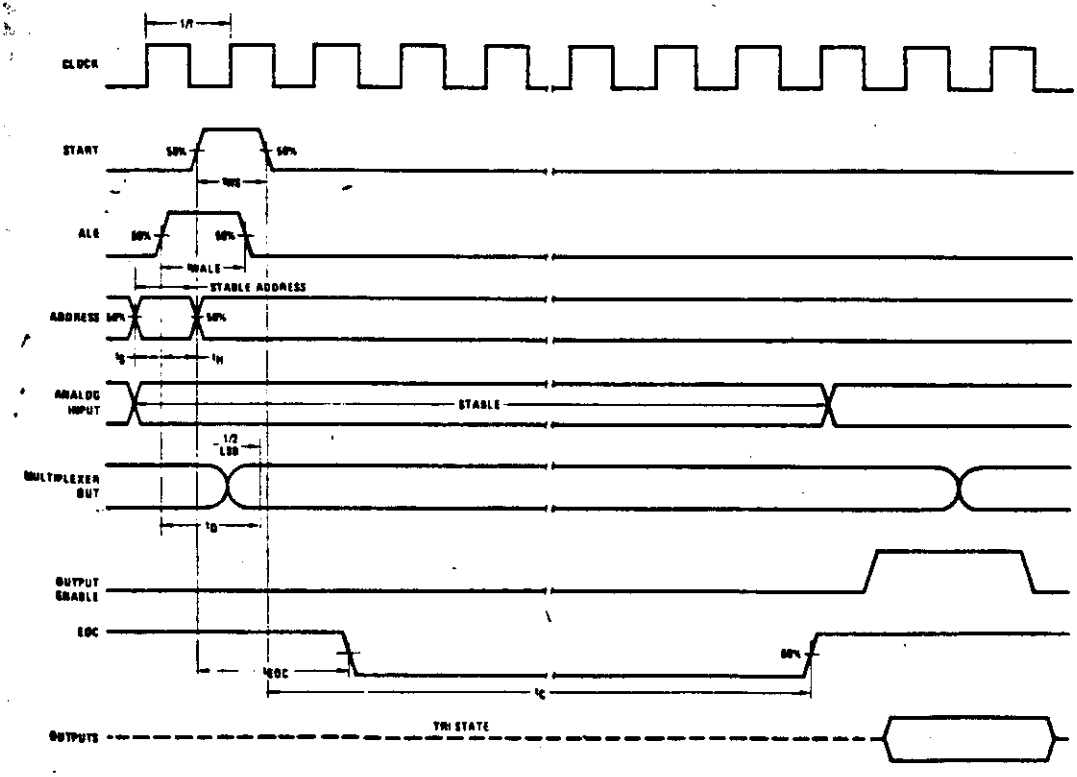


FIGURE 5

Typical Performance Characteristics

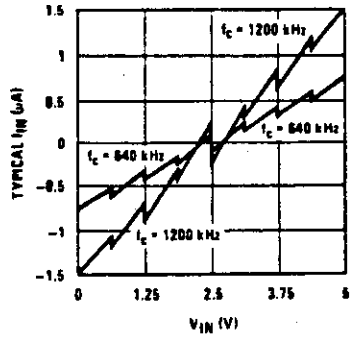


FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

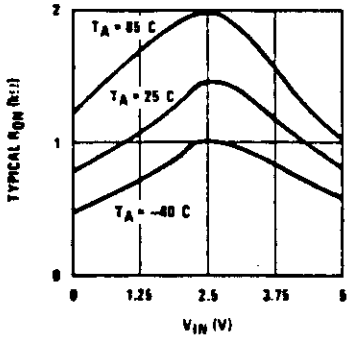


FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE® Test Circuits and Timing Diagrams

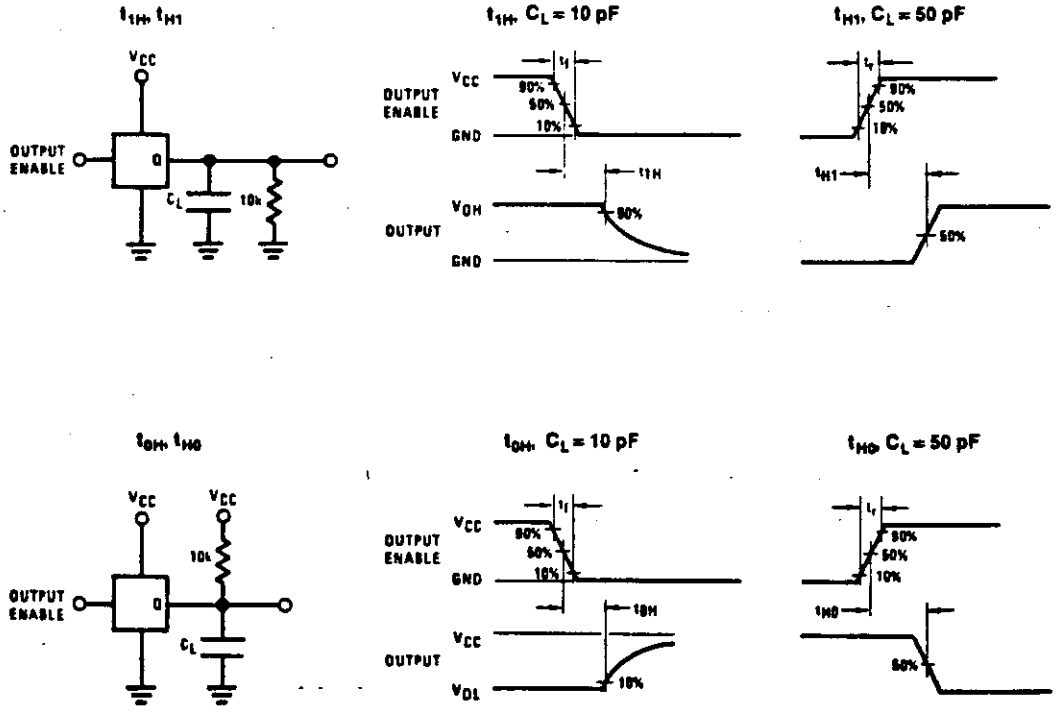
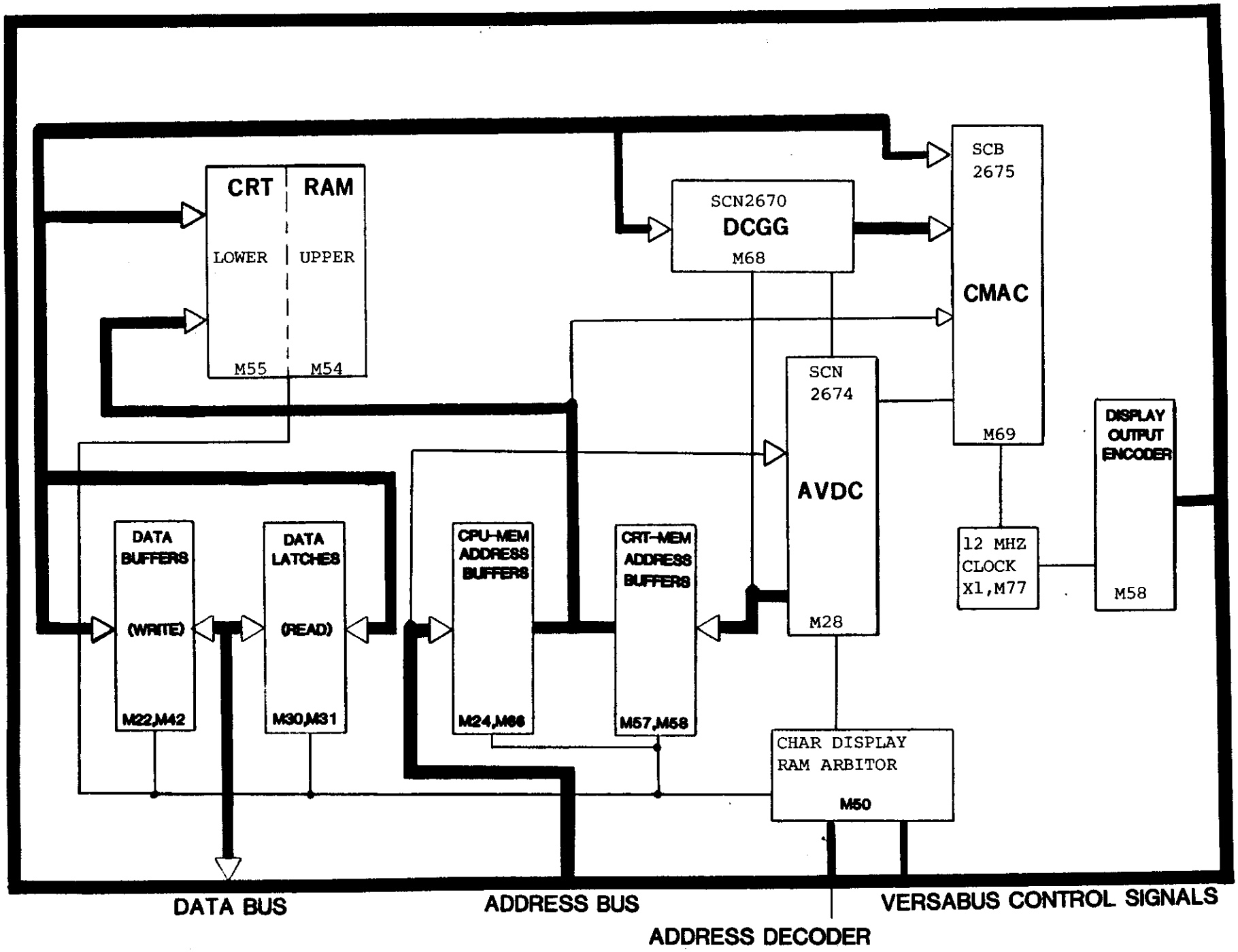


FIGURE 8

BLOCK DIAGRAM- CRT BOARD (DISPLAY GENERATION)



DISPLAY CHARACTER AND GRAPHICS GENERATOR (DCGG) SCN2670

DESCRIPTION

The Signetics Display Character and Graphics Generator (DCGG) is a mask-programmable 11,648-bit line select character generator. It contains 128 10X9 characters placed in a 10X16 matrix, and has the capability of shifting certain characters, such as j, y, g, p and q, that normally extend below the baseline. Character shifting, previously requiring additional external circuitry, is now accomplished internally by the DCGG; effectively, the 9 active lines are lowered within the matrix to compensate for the character's position.

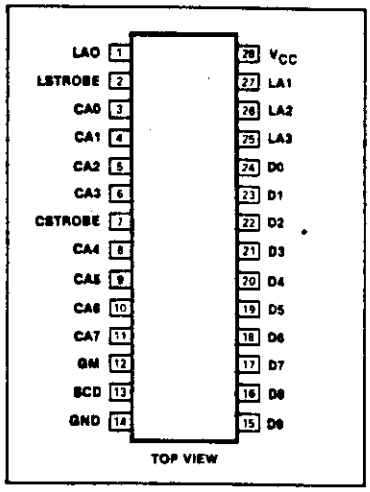
Seven bits of an 8-bit address code are used to select 1 of the 128 available characters. The eighth bit functions as a chip enable signal. Each character is defined by a pattern of logic 1s and 0s stored in a 10X9 matrix. When a specific 4-bit binary line address code is applied, a word of 10 parallel bits appears at the output. The lines can be sequentially selected, providing a 9-word sequence of 10 parallel bits per word for each character selected by the address inputs. As the line address inputs are sequentially addressed, the device will automatically place the 10X9 character in 1 of 2 preprogrammed positions on the 16-line matrix with the positions defined by the 4-line address inputs. One or more of the 10 parallel outputs can be used as control signals to selectively enable functions such as half-dot shift, color selection, etc.

The 2670 DCGG includes latches to store the character address and line address data. A control input to inhibit character data output for certain groups of characters is also provided. The 2670 also includes a graphics capability, wherein the 8-bit character code is translated directly into 256 possible user programmable graphic patterns. Thus, the DCGG can generate data for 384 distinct patterns, of which 128 are defined by the mask programmable ROM. See figure 1 for a typical applications display.

FEATURES

- 128 10X9 matrix characters
- 256 graphic characters
- Optional thin graphics for forms
- Character and line address latches
- Internal descend logic
- 200nsec and 300nsec character select access time versions
- Control character output inhibit logic
- Static operation—no clocks required
- Single 5V power supply
- TTL compatible inputs and outputs

PIN CONFIGURATION

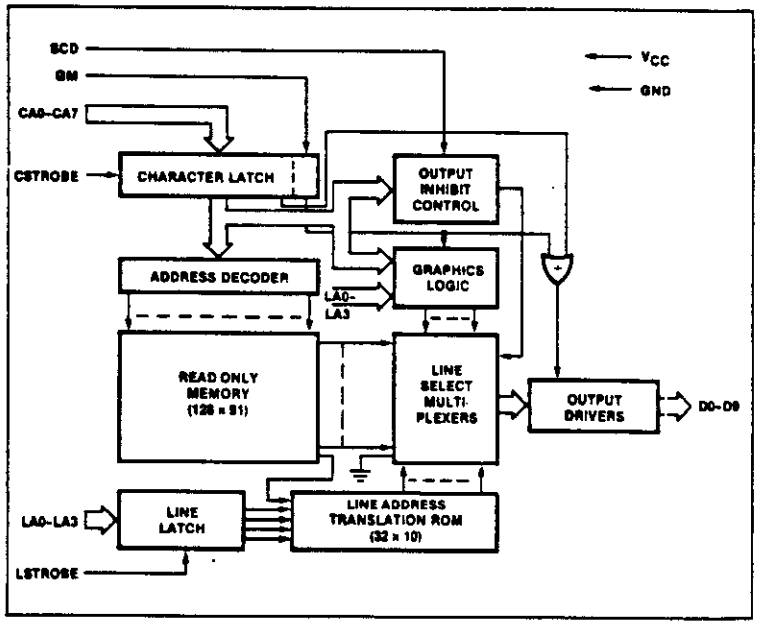


ORDERING CODE

PACKAGES	V_{CC} = 5V ±5%, T_A = 0°C to 70°C	
	t_{CA} = 200ns	t_{CA} = 300ns
Ceramic DIP	SCN2670*C2I28	SCN2670*C3I28
Plastic DIP	SCN2670*C2N28	SCN2670*C3N28

NOTE
Substitute letter corresponding to standard font for "*" in part number for standard parts. See back of data sheet. Contact sales office for custom ROM patterns.

BLOCK DIAGRAM



DISPLAY CHARACTER AND GRAPHICS GENERATOR (DCGG) SCN2670

PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
CA0-CA7	3-6, 8-11	I	**Character Address:** Eight bit code specifies the character or graphic pattern for which matrix data is to be supplied. In character mode (GM=0), CA0 thru CA6 select one of the 128 ROM-defined characters and CA7 is a chip enable. The outputs are active when CA7=1 and are tri-stated when CA7=0. In graphics mode (GM=1), the outputs are active and CA0 thru CA7 select one of 256 possible graphic patterns to be output.
CSTROBE	7	I	**Character Strobe:** Used to store the character address (CA0 thru CA7) and graphics mode (GM) inputs into the character latch. Data is latched on the negative going edge of CSTROBE.
GM	12	I	**Graphics Mode:** GM=0 (low) selects character mode; GM=1 (high) selects graphics mode.
LA0-LA3	1, 25-27	I	**Line Address:** In character mode, selects one of the 16 lines of matrix data for the selected character to appear at the 10 outputs. LA0 is the LSB and LA3 is the MSB. The input codes which cause each of the nine lines of character data to be output are specified as part of the programming data for both non-shifted and shifted fonts. Cycling through the nine specified counts at the LA0 thru LA3 inputs cause successive lines of data to be output on D0 thru D9. The 7 non-specified codes for both non-shifted and shifted characters cause blanks (logic zeros) to be output. In graphics mode, the line address gates the latched graphics data directly to the outputs.
LSTROBE	2	I	**Line Strobe:** Used to store the line address data (LA0 thru LA3) in the line address latch. Data is latched on the negative going edge of LSTROBE.
SCD	13	I	**Selected Character Disable:** In character mode, a high level at this input causes all outputs (regardless of line address) to be blanks (zeros) for characters for which CA6 and CA5 are both 0. A low level input selects normal operation. Inoperative in the graphics mode.
D9-D0	15-24	O	**Data Outputs:** Provide the data for the specified character and line.
V_{CC}	28	I	+5V power supply.
GND	14	I	Ground.

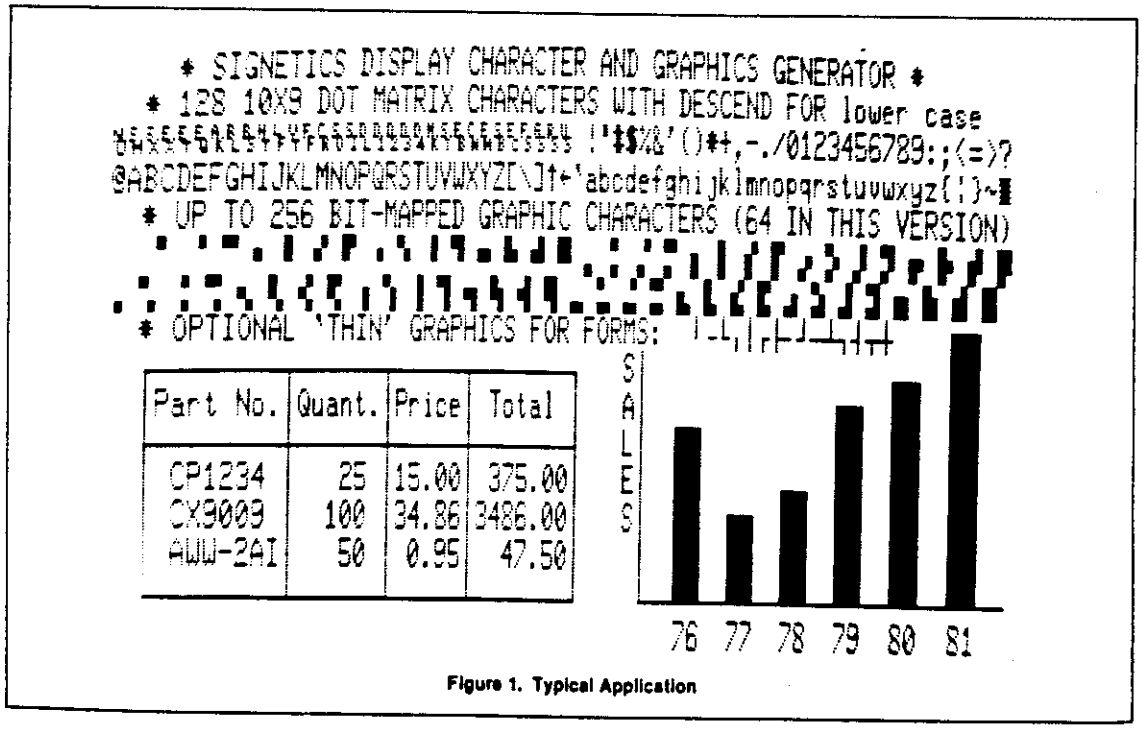


Figure 1. Typical Application

FUNCTIONAL DESCRIPTION

The DCGG consists of nine major sections. Line and character codes are strobed into the line and character latches. The character latch outputs are presented to the three sources of data: the ROM through an address decoder, the graphics logic, and the output inhibit control. The output inhibit control (together with the SCD input) suppresses the ROM data for selected character codes. The outputs from the line latch drive the line address translation ROM which maps the character ROM data onto 9 of 16 line positions. Finally, the line select multiplexers route the ROM or graphics data to the output drivers on D0 through D9.

Character Latch

The character latch is a 9-bit edge triggered latch used to store the character address (CA0 thru CA7) and graphics mode (GM) inputs. The data is stored on the falling edge of CSTROBE. Seven latched addresses (CA0 thru CA6) are inputs to the ROM character address decoder. In character mode (GM=0), CA7 operates as a chip enable. The output drivers are enabled when CA7=1 and are tri-stated when CA7=0. In graphics mode (GM=1), the output drivers are always enabled and the CA0 thru CA7 outputs of the latch are used to generate graphic symbols.

Character Address Decoder

This circuit decodes the 7-bit character address from the character latch to select one of the 128 character fonts stored in the ROM section of the DCGG.

Read Only Memory

The 11,648-bit ROM stores the fonts for the 128 matrix-defined characters. The data for each character consists of 91 bits. Ninety bits represent the 10X9 matrix and one bit specifies whether the character data is output at the normal (unshifted) lines or at the descended (shifted) lines. The 90 data bit outputs are supplied to the line select multiplexers. The descend control bit is an input to the line address translation ROM.

Graphics Logic

When the GM input is zero (low), the DCGG operates in the character mode. When it is one (high), it operates in the graphics mode. In graphics mode, output data is generated by the graphics logic instead of the ROM. The graphics logic maps the latched character address (CA0 thru CA7) to the outputs (D0 thru D9) as a function of line address (LA0 thru LA3). For any particular line address value, two of the CA bits are output: CA0, CA2, CA4 or CA6 is output on D0 thru D4 and CA1, CA3, CA5 or CA7 is output on D5 thru D9. The outputs are paired: When CA0 is output on D0 thru D4, CA1 is output on D5 thru D9 and likewise for CA2-CA3, CA4-CA5 and CA6-CA7.

A ROM within the graphics logic allows the specific line numbers for which each pair of bits is output to be specified by the customer. Figure 2 illustrates the general format for graphics symbols and an example where (CA7 thru CA0) = H'65'. The outputs from the graphics logic go to the line select multiplexers. The multiplexers route the graphic symbol data to the outputs when GM = 1.

Thin Graphics Option

As a customer specified option, 16 of the possible graphic codes (H'60' to H'6F') may be used to generate the special graphic characters illustrated in figure 3. For each of these characters, the vertical component appears on the D4 output. The horizontal component occurs on L_H which is specified by the customer. The vertical components specified by CA0 and CA2 are output for line addresses zero thru L_H and L_H thru fifteen, respectively.

Line Select Multiplexers

The ten line select multiplexers select ROM data as specified by the line address translation ROM when GM=0, or graphics data when GM=1. The inputs to each multiplexer are the nine line outputs from the ROM, an output from the graphics logic and a logic zero (ground).

Output Drivers

Ten output drivers with 3-state capability serve as buffers between the line select multiplexers and external logic. The 3-state control input to these drivers is supplied from the CA7 latch when GM=0. When GM=1, the outputs are always active.

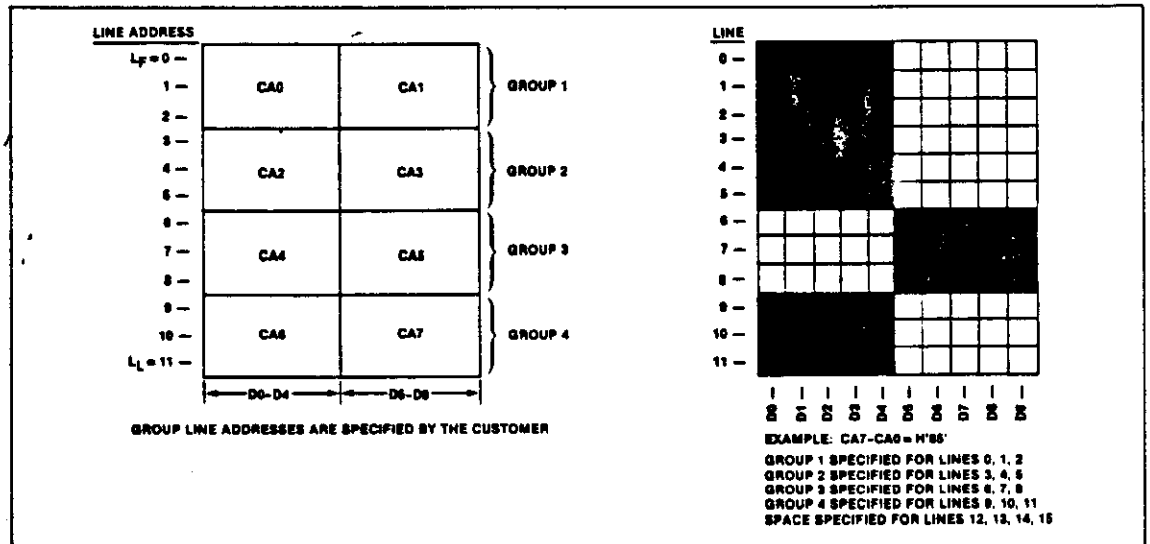


Figure 2. Graphics Symbols — General Format

Output Inhibit Control

The output inhibit control logic operates only if GM=0. It causes the output of the line select multiplexers to be logic zero if the SCD input is high and CA6 and CA5 of the latched character address are 00. If the SCD input is low, normal operation occurs. (This feature is useful in ASCII coded applications to selectively disable character generation for non-displayable characters such as line feed, carriage return, etc.)

Line Address Latch

The line address latch is a 4-bit latch used to store the line address (LA0-LA3). The data is stored on the negative edge of the LSTROBE input.

Line Address Translation ROM

This 32X10 ROM translates the 5-bit code consisting of the 4 outputs from the line address latch and the descend control bit from the ROM into a 1-of-10 code for the line select multiplexers. Programming information provided by the customer specifies the address which selects each line of ROM data for both shifted and non-shifted characters. Thus, there are nine line addresses which select ROM data for unshifted characters and nine addresses for shifted characters. These combinations are usually specified by the customer in either ascending or descending order. For the remaining 14 codes (7 each for unshifted and shifted characters), the translation ROM forces zeros at the outputs of the line select multiplexers.

This circuitry only operates if GM=0. When GM=1, the line select multiplexers are forced to select the outputs from the graphics logic.

Figure 4 shows an example of data outputs where the customer has specified line 14 as the first line for unshifted characters, line 11 as the first line for shifted characters and line address combinations in descending order.

CUSTOM PATTERN PROGRAMMING INSTRUCTIONS

A computer-aided technique utilizing punched computer cards is employed to specify a custom version of the 2670. This technique requires that the customer supply Signetics with a deck of standard 80-column computer cards describing the data to be stored in the ROM array, the programmable line address translation ROM, thin graphics option, and the graphics line font translation ROM.

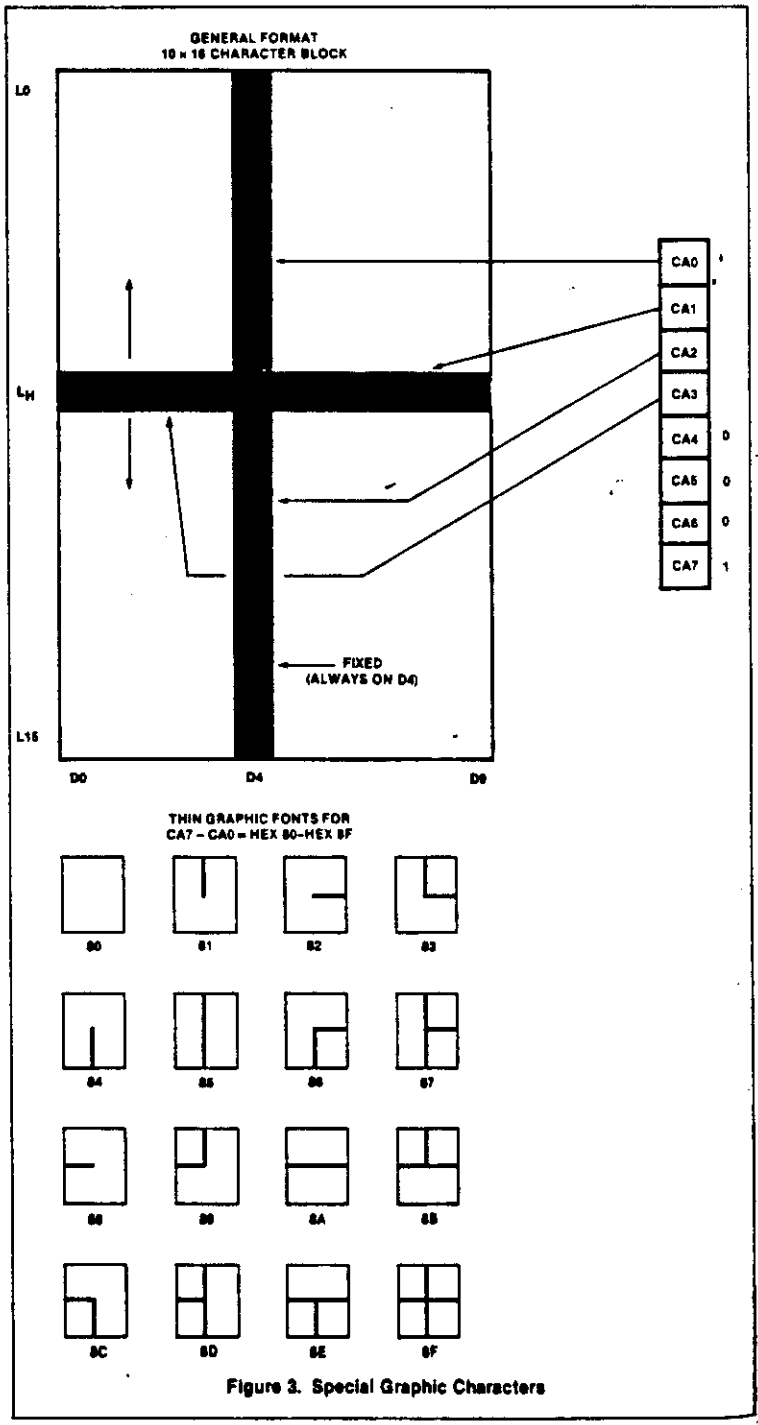


Figure 3. Special Graphic Characters

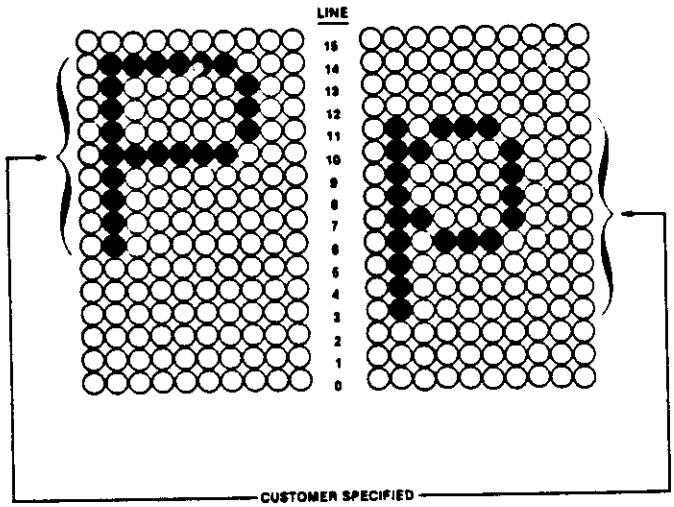


Figure 4. Customer Specified Example

On receipt of a card deck, Signetics will translate the card deck to a truth table using the Signetics Computer Aided Design (CAD) facility. The truth table and font diagrams will then be sent to the customer for final approval. On receipt of final approval, Signetics will produce masks and proceed with manufacturing.

Programming information can also be input on TTY 7-level tape as card images. Each card image must be terminated with a carriage return-line feed. An EOT character must signify the end of the data set.

Customer identification cards are always labeled with a C in column 1. For customer identification, four cards are required. Any number of additional customer identification cards are permitted. The following data should be included:

CUSTOMER ID CARD #1

COLUMN	DATA
1	C
2	blank
3-9	2670/CP
10-14	blank
15-70	Company name/ company part number
71-80	blank

CUSTOMER ID CARD #2

COLUMN	DATA
1	C
2	blank
3-70	Customer contact person name/ phone number
71-80	blank

CUSTOMER ID CARD #3

COLUMN	DATA
1	C
2	blank
3-70	Customer address
71-80	blank

CUSTOMER ID CARD #4

COLUMN	DATA
1	C
2	blank
3-70	Customer city, state, zip code
71-80	blank

CUSTOMER ID CARD #5 THRU N

COLUMN	DATA
1	C
2	blank
3-70	Any information desired
71-80	blank

The following masking information cards must be included:

Mask Information Card #1: Shift and Nonshift Character Translation Data

COLUMN	DATA
1-9	NONSHIFT=
10	Line address in hex which outputs the first font word for nonshifted ROM fonts
11	,
12	Line address in hex which outputs the second font word for nonshifted ROM fonts
13	,
14	third
15	,
16	fourth
17	,
18	fifth
19	,
20	sixth
21	,
22	seventh
23	,
24	eighth
25	,
26	ninth
27-29	blank
30-35	SHIFT=
36	Line address in hex which outputs the first font word for shifted ROM fonts
37	,
38	second
39	,
40	third
41	,
42	fourth
43	,
44	fifth
45	,
46	sixth
47	,
48	seventh
49	,
50	eighth
51	,
52	ninth
53-59	blank
60[1]	0 or 1
61-64	blank
65[2]	0 or 1
66-80	blank

NOTES

1. Column 60 specifies the font truth table horizontal format. 0 specifies left to right printing of D0 thru D9. 1 specifies D9 thru D0.
2. Column 65 specifies the font truth table vertical printout format. 0 specifies top to bottom printing of line address hex 0 thru F. 1 specifies hex F thru 0.

MASK INFORMATION CARD #2: Graphics Translation Data

COLUMN	DATA
1-14	THIN GRAPHICS=
15-17	YES or NO␣, where ␣ = blank. Specifies whether graphics address hex 80 thru hex 8F will select the special thin graphics font.
18-19	blank
20-23	HOR=
24	The line address in hex for the horizontal segments of line graphics fonts. Leave blank if columns 15 thru 17 are NO
25-29	blank
30-45	Graphics group number 1 or 2 or 3 or 4 or blank. Columns 30 thru 45 correspond to line address hex 0 thru hex F respectively. The group number specified in each column will cause the graphics data generated by that group to be output at the corresponding line address. A blank specifies no data for that address.
46-80	blank

MASK INFORMATION CARD #3 THRU #130: ROM Font Data

COLUMN	DATA
1-2	Character address in hex (CA6 thru CA0)*
3	blank
4	S for shifted; N for nonshifted.
5	blank
6-8	Data for first ROM font word in hex (D9 thru D0).
9	blank
10-12	second
13	blank
14-16	third
17	blank
18-20	fourth
21	blank
22-24	fifth
25	blank
26-28	sixth
29	blank
30-32	seventh
33	blank
34-36	eighth
37	blank
38-40	ninth
41-80	blank

NOTE

*A separate card is required for each character address hex 00 thru hex 7F.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Supply voltage	6.0	V
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
All voltages with respect to ground[3]	−0.3 to +6.0	V

NOTES
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 80°C/W junction to ambient (ceramic package).
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless it is suggested that conventional precautions be taken to avoid applying any voltages larger than the maxima.

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% [1,2,3]

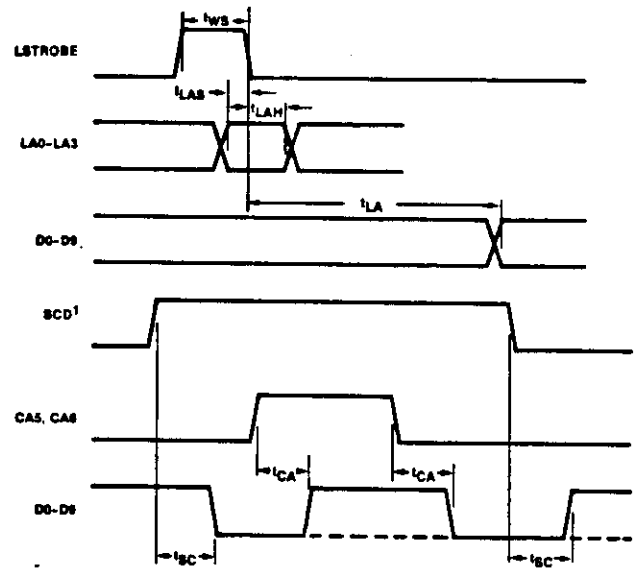
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage		0		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
V_{OL}	Output low voltage	I_O = 1.6mA	0		0.4	V
V_{OH}	Output high voltage	I_O = −100μA	2.4		V_{CC}	V
I_{IL}	Input leakage current	V_{IN} = 0 to 4.25V			10	μA
I_{OL}	Output leakage current	V_O = 0.4 to 4V			± 10	μA
I_{CC}	Supply current	V_{CC} = 5.25V		35	80	mA
C_{IN}	Input capacitance	All other pins grounded			10	pF
C_{OUT}	Output capacitance				15	pF

AC CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ± 5% [1,2,3,4]

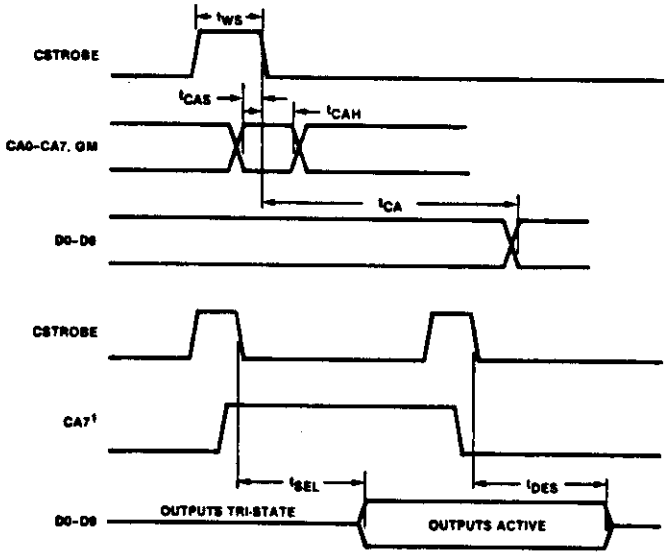
PARAMETER		LIMITS				Unit
		300ns		200ns		
		Min	Max	Min	Max	
t_{WS}	Strobe pulse width	100		100		ns
t_{LAS}	Line address setup	50		50		ns
t_{LAH}	Line address hold	25		25		ns
t_{CAS}	Character address setup	25		15		ns
t_{CAH}	Character address hold	25		15		ns
t_{CA}	Character select access		300		200	ns
t_{LA}	Line select access		500		350	ns
t_{SEL}	Chip select delay		250		150	ns
t_{DES}	Chip deselect delay		200		125	ns
t_{SC}	Special character blank/unblank time		300		200	ns

NOTES
1. Parameters are valid over operating temperature range unless otherwise specified.
2. All voltage measurements are referenced to ground. All time measurements are at the 0.8V or 2.0V level for inputs and outputs. Input levels are 0V and 2.4V.
3. Typical values are at +25°C, typical supply voltages and typical processing parameters.
4. Test conditions: C_L = 100pF and 1 TTL load.

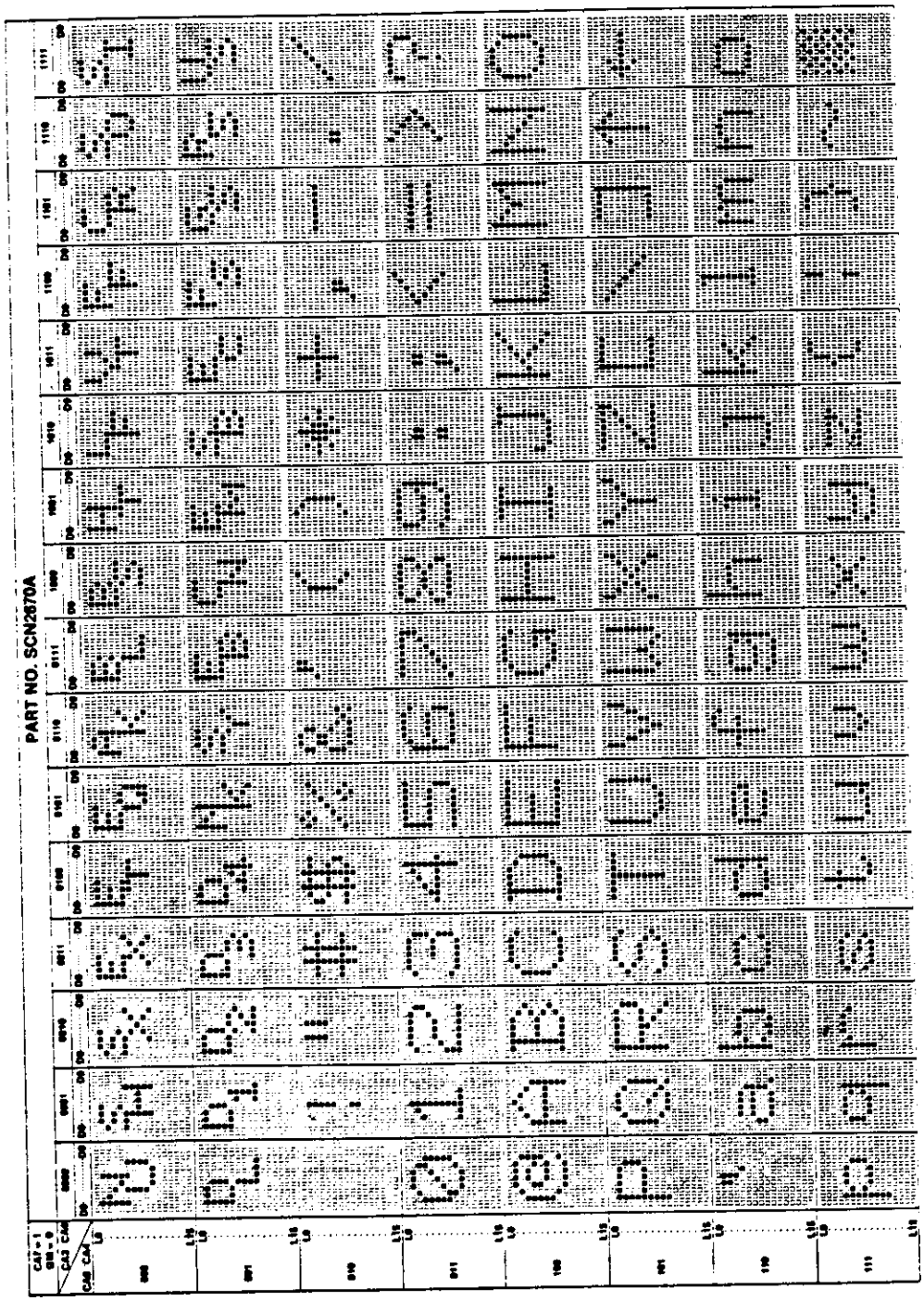
TIMING DIAGRAMS

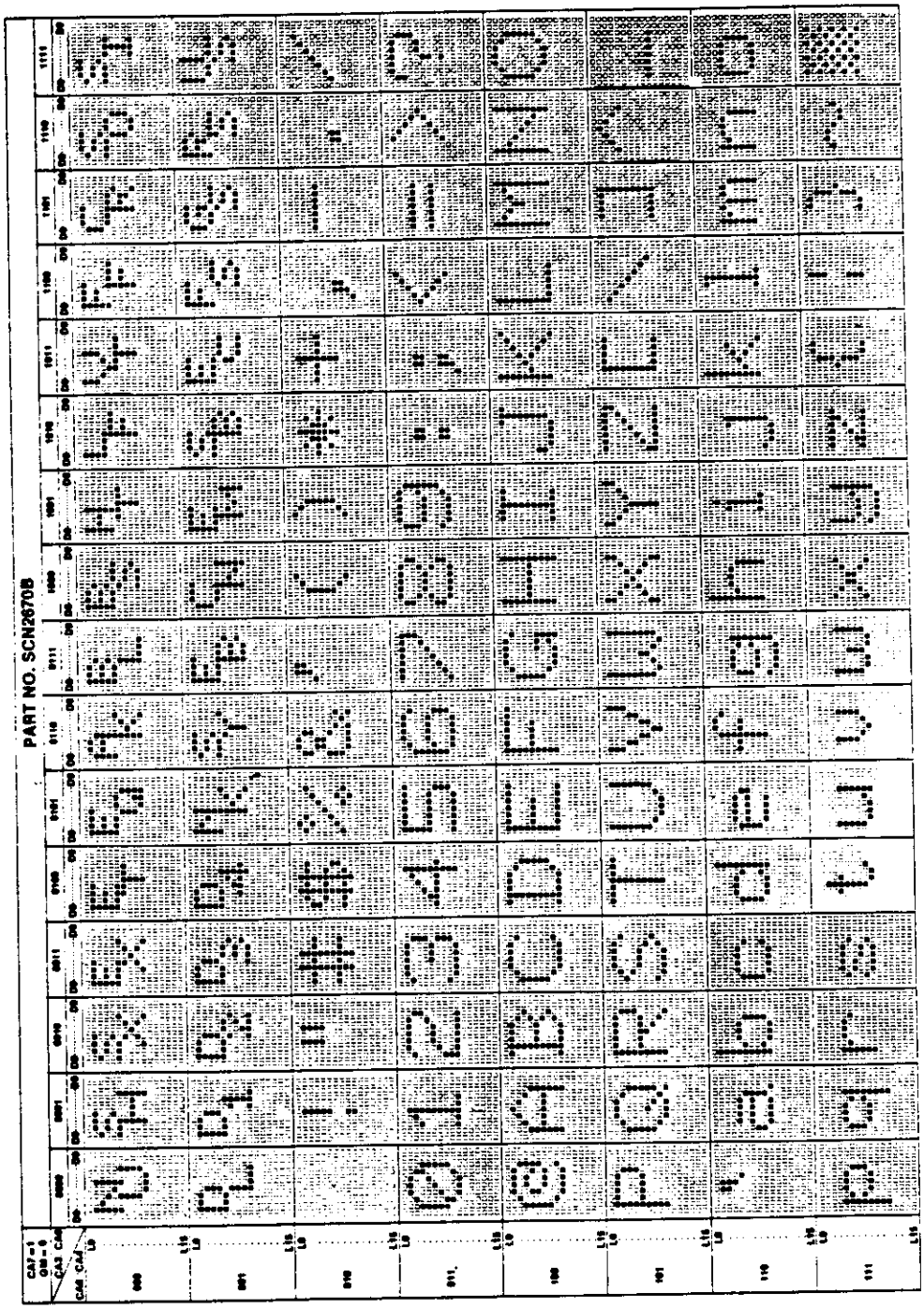


NOTE
1. WHEN GM = 1, SCD INPUT IS INACTIVE



NOTE
1. CA7 OPERATES AS OUTPUT ENABLE ONLY IN CHARACTER MODE (GM = 0)


PART NO. SCN2670A


PART NO. SCN2670B

ADVANCED VIDEO DISPLAY CONTROLLER (AVDC) SCN2674

Preliminary

DESCRIPTION

The Signetics SCN2674 Advanced Video Display Controller (AVDC) is a programmable device designed for use in CRT terminals and display systems that employ raster scan techniques. The AVDC generates the vertical and horizontal timing signals necessary for the display of interlaced or non-interlaced data on a CRT monitor. It provides consecutive addressing to a user specified display buffer memory domain and controls the CPU-display buffer interface for various buffer configuration modes. A variety of operating modes, display formats, and timing profiles can be implemented by programming the control registers in the AVDC.

A minimum CRT terminal system configuration consists of an AVDC, an SCN2671 Keyboard and Communication Controller (PKCC), an SCN2670 Display Character and Graphics Generator (DCGG), an SCB2675 Color/Monochrome Attributes Controller (CMAC), a single chip microcomputer such as the 8048, a display buffer RAM, and a small amount of TTL for miscellaneous address decoding, interface, and control. Typically, the package count for a minimum system is between 15 and 20 devices; system complexity can be enhanced by upgrading the microprocessor and expanding via the system address and data busses.

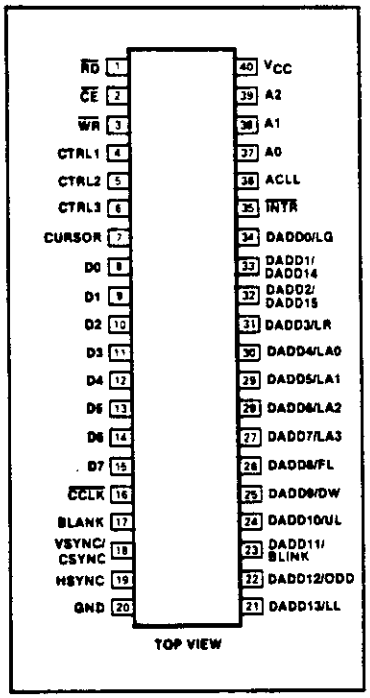
FEATURES

- 4MHz character rate
- 1 to 256 characters per row
- 1 to 16 raster lines per character row
- 1 to 128 character rows per frame
- Bit mapped graphics mode
- Programmable horizontal and vertical sync generators
  - RS170 compatible sync
- Interlaced or non-interlaced operation
- Up to 64K RAM addressing for multiple page operation
- Readable, writable and incrementable cursor
  - Programmable cursor size and blink
- AC line lock
- Automatic wraparound of RAM
- Automatic split screen
- Automatic bidirectional soft scrolling
  - Programmable scan line increment
- Row table addressing mode
- Double height tops and bottoms
- Double width control output
- Selectable buffer interface modes
- Dynamic RAM refresh
- Completely TTL compatible
- Single +5 volt power supply
- Power on reset circuit

APPLICATIONS

- CRT terminals
- Word processing systems
- Small business computers
- Home computers

PIN CONFIGURATION



2

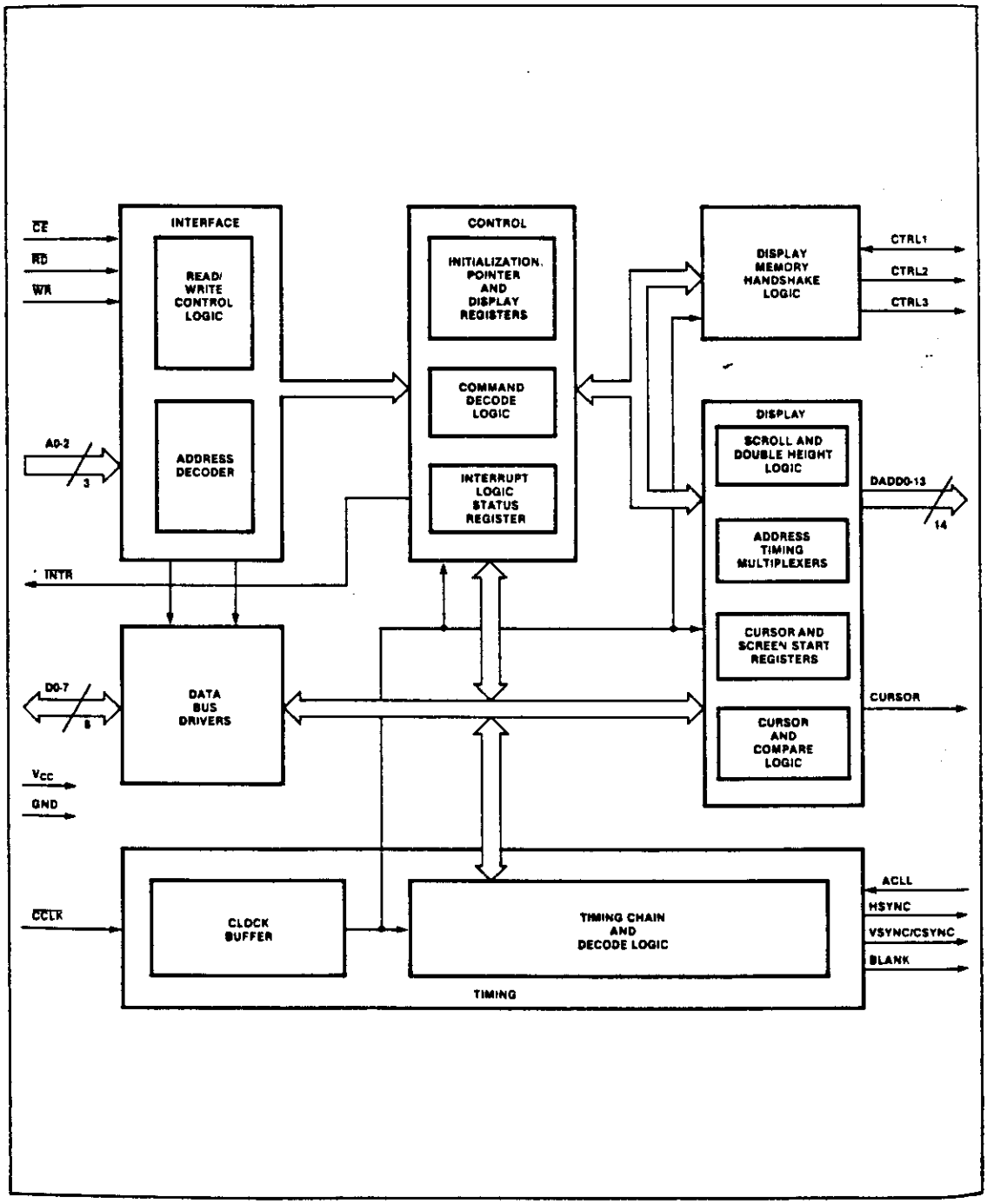
ORDERING CODE

PACKAGES	V_{CC} = 5V ± 5%, T_A = 0° to 70°C	
	4MHz	2.7MHz
Ceramic DIP	SCN2674BC4I40	SCN2674BC3I40
Plastic DIP	SCN2674BC4N40	SCN2674BC3N40

ADVANCED VIDEO DISPLAY CONTROLLER (AVDC) SCN2674

Preliminary

BLOCK DIAGRAM



ADVANCED VIDEO DISPLAY CONTROLLER (AVDC)

SCN2674

Preliminary

PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
A0-A2	37-39	I	**Address Lines:** Used to select AVDC internal registers for read/write operations and for commands.
D0-D7	8-15	I/O	**8-Bit Bidirectional Three-State Data Bus:** Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the AVDC take place over this bus. The direction of the transfer is controlled by the $\overline{RD}$ and $\overline{WR}$ inputs when the $\overline{CE}$ input is low. When the $\overline{CE}$ input is high, the data bus is in the three-state condition.
$\overline{RD}$	1	I	**Read Strobe:** Active low input. A low on this pin while $\overline{CE}$ is low causes the contents of the register selected by A0-A2 to be placed on the data bus. The read cycle begins on the leading (falling) edge of $\overline{RD}$.
$\overline{WR}$	3	I	**Write Strobe:** Active low input. A low on this pin while $\overline{CE}$ is also low causes the contents of the data bus to be transferred to the register selected by A0-A2. The transfer occurs on the trailing (rising) edge of $\overline{WR}$.
$\overline{CE}$	2	I	**Chip Enable:** Active low input. When low, data transfers between the CPU and the AVDC are enabled on D0-D7 as controlled by the $\overline{WR}$, $\overline{RD}$, and A0-A2 inputs. When $\overline{CE}$ is high, effectively, the AVDC is isolated from the data bus and D0-D7 are placed in the three-state condition.
$\overline{CCLK}$	16	I	**Character Clock:** Timing signal derived from the video dot clock which is used to synchronize the AVDC's timing functions.
HSYNC	19	O	**Horizontal Sync:** Active high output which provides video horizontal sync pulses. The timing parameters are programmable.
VSYNC/CSYNC	18	O	**Vertical Sync/Composite Sync:** A control bit selects either vertical or composite sync pulses on this active high output. When CSYNC is selected, equalization pulses are included. The timing parameters are programmable.
BLANK	17	O	**Blank:** This active high output defines the horizontal and vertical borders of the display. Display control signals which are output on DADD0 and DADD3 thru DADD13 are valid on the trailing edge of BLANK.
CURSOR	7	O	**Cursor Gate:** This output becomes active for a specified number of scan lines when the address contained in the cursor register matches the address output on DADD0 through DADD13 for displayable character addresses. The first and last lines of the cursor and a blink option are programmable. When the row table addressing mode is enabled, this output is active for a portion of the blanking interval prior to the first scan line of a character row, while the AVDC is fetching the starting address for that row.
$\overline{INTR}$	35	O	**Interrupt Request:** Open drain output which supplies an active low interrupt request from any of five maskable sources. This pin is inactive after a power on reset or a master reset command.
ACLL	36	I	**AC Line Lock:** If this input is low after the programmed vertical front porch interval, the vertical front porch will be lengthened by increments of horizontal scan line times until this input goes high.
CTRL1	4	I/O	**Handshake Control 1:** In independent mode, provides an active low write data buffer ($\overline{WDB}$) output which strobes data from the interface latch into the display memory. In transparent and shared modes, this is an active low processor bus request ($\overline{PBREQ}$) input which indicates that the CPU desires to access the display memory.
CTRL2	5	O	**Handshake Control 2:** In independent mode, provides an active low read data buffer ($\overline{RDB}$) output which strobes data from the display memory into the interface latch. In transparent and shared modes, this is an active low bus external enable ($\overline{BEXT}$) output which indicates that the AVDC has relinquished control of the display memory (DADD0-DADD13 are in the three-state condition) in response to a CPU bus request. $\overline{BEXT}$ also goes low in response to a 'display off and float DADD' command. In row buffer mode, it is an active low bus request ($\overline{BREQ}$) output which halts the CPU during a line DMA.
CTRL3	6	O	**Handshake Control 3:** In independent mode, provides the active low buffer chip enable ($\overline{BCE}$) signal to the display memory. In transparent and shared modes, provides an active low bus acknowledge ($\overline{BACK}$) output which serves as a ready signal to the CPU in response to a processor bus request. In row buffer mode, this is an active high memory bus control (MBC) output which configures the system for the DMA transfer of one row of character codes from system memory to the row display buffer.

ADVANCED VIDEO DISPLAY CONTROLLER (AVDC) SCN2674

Preliminary

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DADD0-DADD13	34-21	O	**Display Address:** Used by the AVDC to address up to 16K of display memory directly, or to 64K of memory by de-multiplexing DADD14 and DADD15. These outputs are floated at various times depending on the buffer mode. Various control signals are multiplexed on DADD0 through DADD13 and are valid at the trailing edge of BLANK. These control signals are: DADD0/LG **Line Graphics:** Output which denotes bit mapped graphics mode. DADD1/DADD14 **Display Address 14:** Multiplexed address bit used to extend addressing to 64K. DADD2/DADD15 **Display Address 15:** Multiplexed address bit used to extend addressing to 64K. DADD3/LR **Last Row:** Output which indicates the last active character row of each field. DADD4-DADD7/LA0-LA3 **Line Address:** Provides the number of the current scan line count for each character row. DADD8/FL **First Line:** Asserted during the blanking interval just prior to the first scan line of each character row. DADD9/DW **Double Width:** Output which denotes a double width character row. DADD10/UL **Underline:** Asserted during the blanking interval just prior to the scan line which matches the programmed underline position (line 0 thru 15). DADD11/BLINK **Blink Frequency:** Provides an output divided down from the vertical sync rate. DADD12/ODD **Odd Field:** Active high signal which is asserted before each scan line of the odd field when interlace is specified. Replaces DADD4/LA0 as the least significant line address for interlaced sync and video applications. DADD13/LL **Last Line:** Asserted during the blanking interval just prior to the last scan line of each character row.
V_{CC}	40	I	**Power Supply:** + 5 volts power input.
GND	20	I	**Ground:** Signal and power ground input.

FUNCTIONAL DESCRIPTION

As shown in the block diagram, the AVDC contains the following major blocks:

- Data bus buffer
- Interface Logic
- Operation Control
- Timing
- Display Control
- Buffer Control

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data busses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the AVDC.

Interface Logic

The interface logic contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are shown in table 1.

Operation Control

The operation control section decodes configuration and operation commands from the CPU and generates appropriate

Table 1 AVDC ADDRESSING

A2	A1	A0	READ ($\overline{RD}$ = 0)	WRITE ($\overline{WR}$ = 0)
0	0	0	Interrupt register	Initialization registers[1]
0	0	1	Status register	Command register
0	1	0	Screen start 1 lower register	Screen start 1 lower register
0	1	1	Screen start 1 upper register	Screen start 1 upper register
1	0	0	Cursor address lower register	Cursor address lower register
1	0	1	Cursor address upper register	Cursor address upper register
1	1	0	Screen start 2 lower register	Screen start 2 lower register
1	1	1	Screen start 2 upper register	Screen start 2 upper register

[1]There are 15 initialization registers which are accessed sequentially via a single address. The AVDC maintains an internal pointer to these registers which is incremented after each write at this address until the last register (IR14) is accessed. The pointer then continues to point to IR14 for additional accesses. Upon a power-on or a master reset command, the internal pointer is reset to point to the first register (IR0) of the initialization register group. The internal pointer can also be preset to any register of the group via the 'load IR address pointer' command

ADVANCED VIDEO DISPLAY CONTROLLER (AVDC) SCN2674

Preliminary

signals to other internal sections to control the overall device operation. It contains the timing and display registers which configure the display format and operating mode, the interrupt logic, and the status register which provides operational feedback to the CPU.

Timing

The timing section contains the counters and decoding logic necessary to generate the monitor timing outputs and to control the display format. These timing parameters are selected by programming of the initialization registers.

Display Control

The display control section generates linear addressing for up to 16K bytes of display memory. Internal comparators limit the portion of the memory which is displayed to programmed values. Additional functions performed in this section include cursor positioning and address comparisons required for generation of timing signals, double height tops and bottoms, smooth scrolling, and the split screen interrupts.

Buffer Control

The buffer control section generates three signals which control the transfer of data between the CPU and the display buffer memory. Four system configurations requiring four different 'handshaking' schemes are supported. These are described below.

SYSTEM CONFIGURATIONS

Figure 1 illustrates the block diagram of a typical display terminal using the Signetics SCN2670, SCN2671, SCN2674, and SCB2675 CRT terminal devices. In this system, the CPU examines inputs from the data communications line and the keyboard and places the data to be displayed in the display buffer memory. This buffer is typically a RAM which holds the data for a single or multiple screenload (page) or for a single character row.

The AVDC supports four common system configurations of display buffer memory, designated the independent, transparent, shared, and row buffer modes. The first three modes utilize a single or multiple page RAM and differ primarily in the means used to transfer display data between the RAM and the CPU. The row buffer mode makes use of a single row buffer (which can be a shift register or a small RAM) that is updated in real time to contain the appropriate display data.

The user programs bits 0 and 1 of IR0 to select the mode best suited for the system environment. The CNTRL1-3 outputs perform different functions for each mode and are named accordingly in the description of each mode.

Independent Mode

The CPU to RAM interface configuration for this mode is illustrated in figure 2. Transfer of data between the CPU and display memory is accomplished via a bidirectional latched port and is controlled by read data buffer ($\overline{RDB}$), write data buffer ($\overline{WDB}$), and buffer chip enable ($\overline{BCE}$). This mode provides a non-contention type of operation that does not require address multiplexers. The CPU does not address the memory directly—the read or write operation is performed at the address contained in the cursor address register or the pointer address register as specified by the CPU. The AVDC enacts the data transfers during blanking intervals in order to prevent visual disturbances of the displayed data.

The CPU manages the data transfers by supplying commands to the AVDC. The commands used are:

1. Read/write at pointer address.
2. Read/write at cursor address (with optional increment of address).
3. Write from cursor address to pointer address.

The operational sequence for a write operation is:

1. CPU checks RDFLG status bit to assure that any delayed commands have been completed.
2. CPU loads data to be written to display memory into the interface latch.
3. CPU writes address into cursor or pointer registers.
4. CPU issues 'write at cursor with/without increment' or 'write at pointer' command.
5. AVDC generates control signals and outputs specified address to perform requested operation. Data is copied from the interface latch into the memory.
6. AVDC sets RDFLG status to indicate that the write is completed.

Similarly, a read operation proceeds as follows:

1. Steps 1 and 3 as above.
2. CPU issues 'read at cursor with/without increment' or 'read at pointer' command.
3. AVDC generates control signals and outputs specified address to perform requested operation. Data is copied from memory to the interface latch and AVDC sets RDFLG status to indicate that the read is completed.
4. CPU checks RDFLG status to see if operation is completed.
5. CPU reads data from interface latch.

Loading the same data into a block of display memory is accomplished via the 'write from cursor to pointer' command:

1. CPU checks RDFLG status bit to assure that any delayed commands have been completed.
2. CPU loads data to be written to display memory into the interface latch.
3. CPU writes beginning address of memory block into cursor address register and ending address of block into pointer address register.
4. CPU issues 'write from cursor to pointer' command.
5. AVDC generates control signals and outputs block addresses to copy data from the interface latch into the specified block of memory.
6. AVDC sets RDFLG status to indicate that the block write is completed.

Similar sequences can be implemented on an interrupt driven basis using the READY interrupt output to advise the CPU that a previously asserted delayed command has been completed.

Two timing sequences are possible for the 'read/write at cursor/pointer' commands. If the command is given during the active display window (defined as first scan line of the first character row to the last scan line of the last character row), the operation takes place during the next horizontal blanking interval, as illustrated in figure 3. If the command is given during the vertical blanking interval, or while the display has been commanded blanked, the operation takes place immediately. In the latter case, the execution time for the command is approximately five character clocks (see figure 4).

Timing for the 'write from cursor to pointer' operation is shown in figure 5. The memory is filled at a rate of one location per two character times. The command will execute only during blanking intervals and may require many horizontal or vertical blanking intervals to complete. Additional delayed commands can be asserted immediately after this command has completed.

Immediate commands can be asserted at any time regardless of the state of the ready status/interrupt.

ADVANCED VIDEO DISPLAY CONTROLLER (AVDC) SCN2674

Preliminary

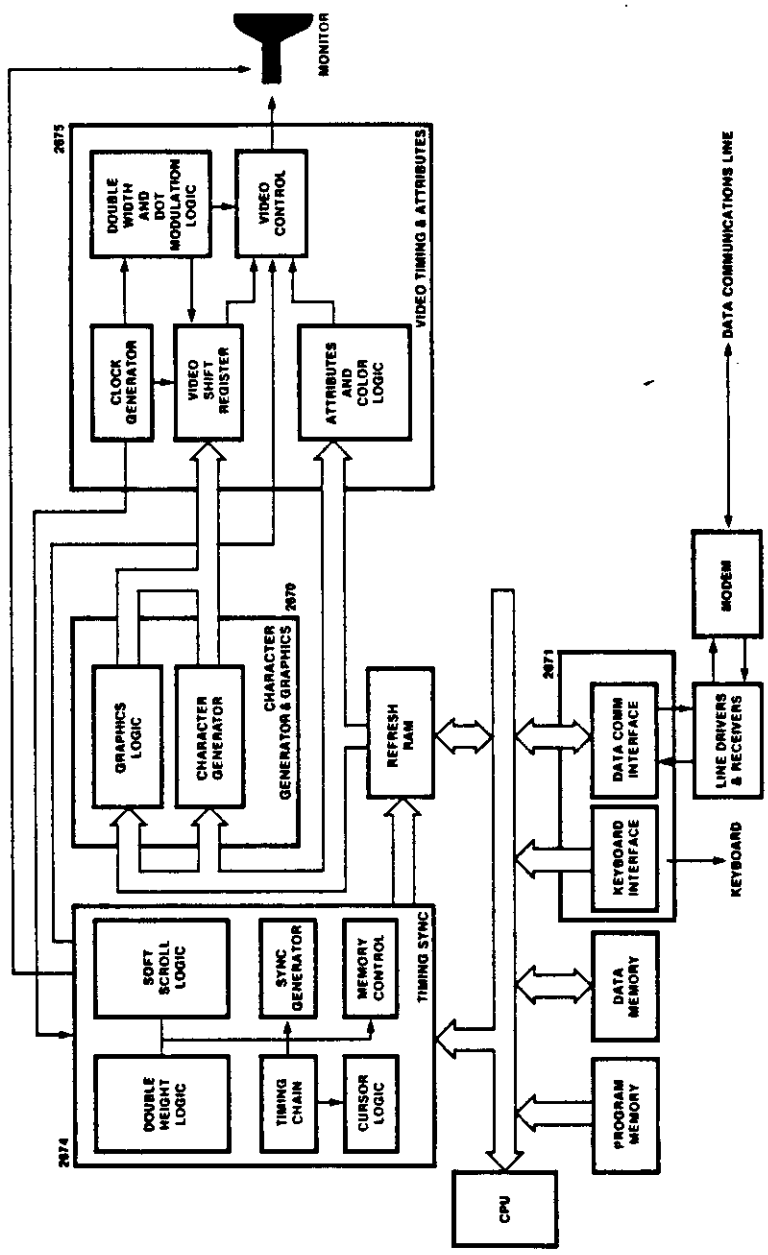


Figure 1. CRT Terminal Block Diagram

COLOR/MONOCHROME ATTRIBUTES CONTROLLER (CMAC) SCB2675

Preliminary

DESCRIPTION

The Signetics SCB2675 Color/Monochrome Attributes Controller (CMAC) is a bipolar LSI device designed for CRT terminals and display systems that employ raster scan techniques. It contains a programmable dot clock divider to generate a character clock, a high speed shift register to serialize input dot data into a video stream, latches and logic to apply visual attributes to the resulting display, and logic to display a cursor on the display.

The CMAC provides control of visual attributes on a character by character basis for two operating modes: monochrome and color. The monochrome mode provides reverse video, blank, highlight and two general purpose user definable attributes. In this mode, the display characters can be specified to appear on either a light or dark screen background. Retrace video suppression can be automatically or externally controlled. The color mode provides eight colors for foreground (character) video and eight colors for background video together with a luminance output for external color set selection or to simultaneously drive a monochrome monitor. Additionally, both modes provide double width, underline, blink, dot stretching and dot width attributes. In monochrome mode, the SCB2675 emulates the attribute characteristics of Digital Equipment Corporation's VT100 terminal.

The horizontal dot frequency is the basic timing input to the CMAC. This clock is divided internally to provide a character clock output for system synchronization. Up to ten bits of dot data are parallel loaded into the video shift register on each character boundary. The two TTL video data outputs in monochrome mode are encoded to provide four video intensities (black, gray, white and highlight). The video data in color mode is encoded to provide eight foreground colors and shifted out on three TTL outputs, together with the luminance output.

FEATURES

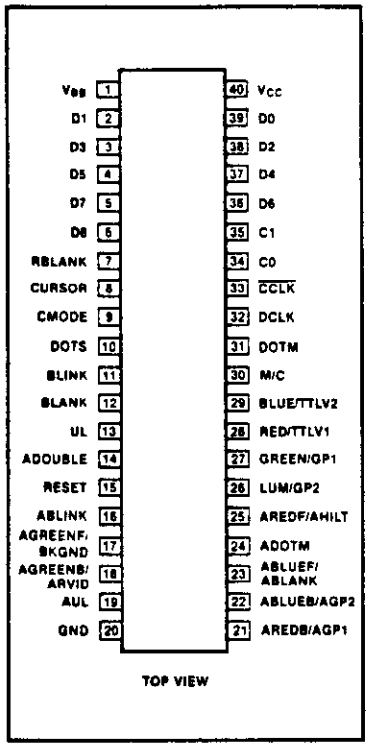
- 25 and 18MHz video dot rate versions*
- Four video intensities encoded on two TTL outputs (monochrome mode)
- Eight foreground and background colors encoded on three TTL outputs (color mode)
- Internally latched character attributes:
  - Reverse video
  - Blank
  - Blink
  - Underline
  - Highlight
  - Two general purpose
  - Eight foreground colors
  - Eight background colors
  - Dot width control
  - Double width characters
- VT100 compatible attributes
- Reverse video cursor with optional white cursor in color mode
- Up to 10 dots per character
- Light or dark background in monochrome mode
  - Automatic retrace blanking
- Programmable dot stretching
- Compatible with SCN2674 AVDC and SCN2670 DCGG
- TTL compatible
- 40-pin dual in-line package

APPLICATIONS

- CRT terminals
- Word processing systems
- Small business computers

*For faster versions consult factory.

PIN CONFIGURATION



TOP VIEW

ORDERING CODE

PACKAGES	DOTS PER CHARACTER	V_{CC} = 5V ± 5%, 0°C to +70°C	
		25MHz	18MHz
Ceramic DIP Plastic DIP	7, 8, 9, 10	SCB2675BC5I40 SCB2675BC5N40	SCB2675BC8I40 SCB2675BC8N40
Ceramic DIP Plastic DIP	6, 8, 9, 10	SCB2675CC5I40 SCB2675CC5N40	SCB2675CC8I40 SCB2675CC8N40

COLOR/MONOCHROME ATTRIBUTES CONTROLLER (CMAC) SCB2675

Preliminary

PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
V_{CC}	40	I	**Power Supply:** + 5VDC
V_{BB}	1	I	**Bias Supply:** See figure 5
GND	20	I	**Ground:** 0V reference
DCLK	32	I	**Dot Clock:** Dot frequency input. Video output shift rate.
$\overline{CCLK}$	33	O	**Character Clock:** An output which is a submultiple of DCLK. The period ranges from 7 to 10 DCLK periods per cycle and is determined by the state of the C0-C1 inputs.
RED/TTLV1	28	O	**Red/TTL Video 1:** In color mode, this output provides the red gun serial video. In monochrome mode, it should be used with the blue/TTL video 2 output to decode four video intensities.
BLUE/TTLV2	29	O	**Blue/TTL Video 2:** In color mode, this output provides the blue gun serial video. In monochrome mode, it should be used with the red/TTL video 1 output to decode four video intensities.
GREEN/GP1	27	O	**Green/General Purpose 1:** In color mode, this output provides the green gun serial video. In monochrome mode, it is a general purpose TTL output which is asserted if the AREDB/AGP1 input is asserted when the corresponding character dot data is loaded into the video shift register.
LUM/GP2	26	O	**Luminance/General Purpose 2:** In color mode, this output is the logical-OR of the RGB foreground video. It is low during a blanking interval and during the foreground portion of the cursor display. In monochrome mode, it is a general purpose TTL output which is asserted if the ABLUEB/AGP2 input is asserted when the corresponding character dot data is loaded into the video shift register.
UL	13	I	**Underline Timing:** Indicates the scan line(s) for the underline attribute. Latched on the falling edge of BLANK.
BLINK	11	I	**Blink Timing:** This input is sampled on the falling edge of BLANK to provide the blink rate for the blink attribute. Should be a submultiple of the frame rate.
BLANK	12	I	**Screen Blank:** When high, this input forces the video outputs to the specified background color in color mode and to the level specified by the BKGND input (either black or gray) in monochrome mode.
RBLANK	7	I	**Retrace Blank:** This input is used to force the video outputs to a low during retrace periods. If pulled high, it will automatically suppress video during the retrace periods when BLANK is high. The user may also pulse this input while BLANK is high to selectively suppress raster video.
AGREENF/BKGND	17	I	**Green Foreground/Background Intensity:** In color mode, this input activates the GREEN/GP1 output during the foreground (character video) portion of the associated character block. In monochrome mode, this input specifies gray or black screen background.
ABLUEF/ABLANK	23	I	**Blue Foreground/Blank Attribute:** In color mode, this input activates the BLUE/TTLV2 output during the foreground (character video) portion of the associated character block. In monochrome mode, this input generates a blank space for the associated character. The blank space intensity is controlled by the AGREENF/BKGND input, the reverse video attribute and cursor input.
AREDF/AHILT	25	I	**Red Foreground/Highlight Attribute:** In color mode, this input activates the RED/TTLV1 output during the foreground (character video) portion of the associated character block. In monochrome mode, this input highlights the associated character (including underline).
CURSOR	8	I	**Cursor Timing:** This input provides the timing for the cursor video. In color mode, with CURSOR and CMODE high, the RGB outputs are driven high (white cursor). If CMODE is low, or in monochrome mode, this input reverses the intensities of the video and attributes. Cursor position, shape, and blink rate are controlled by this input.
CMODE	9	I	**Cursor Mode:** Used in color mode only. When CURSOR and CMODE are high, the RGB outputs are driven high (white cursor). When CURSOR is high and CMODE is low, the RGB outputs are logically inverted (reverse video cursor).
AUL	19	I	**Underline Attribute:** Specifies a line to be displayed in the character block. The specific line(s) are specified by the UL input. All other attributes apply to the underline video.

COLOR/MONOCHROME ATTRIBUTES CONTROLLER (CMAC) SCB2675

Preliminary

PIN DESIGNATION (Continued)

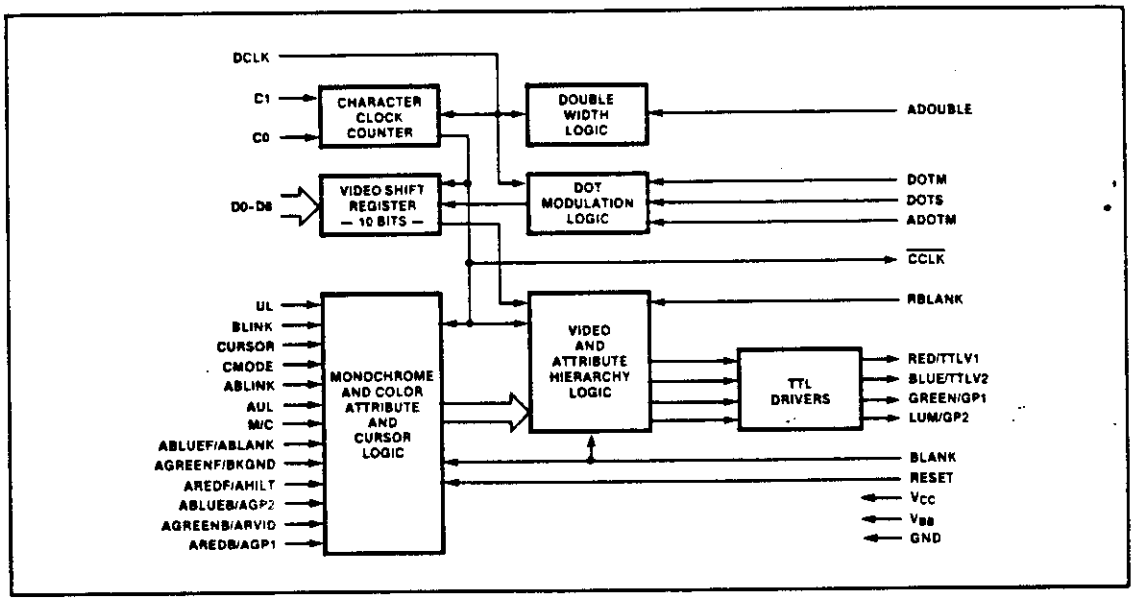
MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
ABLINK	16	I	**Blink Attribute:** In color mode, this active high input will drive the foreground RGB combination to the background RGB combination. In monochrome mode, the associated character or background is driven to the intensity determined by BKGND, reverse video attribute and the cursor input.
ADOUBLE	14	I	**Double Width Attribute:** This active high input causes the associated character video to be shifted out of the serial shift register at one half the dot frequency (DCLK). The $\overline{CCLK}$ output is not affected.
AREDB/AGP1	21	I	**Red Background/General Purpose Attribute 1:** In color mode, this input activates the RED/TTLV1 output during the background portion of the associated character block. In monochrome mode, it activates the GREEN/GP1 output for the associated character block.
ABLUEB/AGP2	22	I	**Blue Background/General Purpose Attribute 2:** In color mode, this input activates the BLUE/TTLV2 output during the background portion of the associated character block. In monochrome mode, it activates the LUM/GP2 output for the associated character block.
AGREENB/ARVID	18	I	**Green Background/Reverse Video Attribute:** In color mode, this input activates the GREEN/GP1 output during the background portion of the associated character block. In monochrome mode, it causes the associated character block video intensities to be reversed.
D0-D8	36-39, 2-6	I	**Dot Data Input:** These are parallel inputs corresponding to the character/graphic symbol dot data for a given scan line. These inputs are strobed into the video shift register on the trailing (falling) edge of each character clock ($\overline{CCLK}$).
C0-C1	34-35	I	**Character Clock Control:** The states of these two static inputs determine the internal divide factor for the $\overline{CCLK}$ output rate.
RESET	15	I	**Reset:** This active high input initializes the internal logic and resets the attribute latches.
M/C	30	I	**Monochrome/Color Mode:** This input selects whether the CMAC operates in monochrome or color mode. A low selects color mode and a high selects monochrome mode.
ADOTM	24	I	**Dot Modulation Attribute:** When DOTM and this input are high, the active dot width of the associated character video is one DCLK. When DOTM is high and this input is low, the active dot width of the associated character video is two DCLKs.
DOTM	31	I	**Dot Width Modulation:** When this input is high, two DCLKs are used for each dot shifted through the shift register. When this input is low, one DCLK is used.
DOTS	10	I	**Dot Stretching:** Sampled at the falling edge of BLANK. When this input is high, one extra dot is appended to individual dots or groups of dots of the input parallel data and then transferred through the shift register. When this input is low, normal transfer of input parallel data results.

2

COLOR/MONOCHROME ATTRIBUTES CONTROLLER (CMAC) SCB2675

Preliminary

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The CMAC consists of seven major sections (see block diagram). The high speed dot clock input is applied to a programmable divider to provide a character clock output for system timing. Parallel dot data is loaded into the video shift register on character boundaries and shifted into the video logic block at the dot rate specified by the dot modulation section. The appropriate attribute control inputs are selected by the mode select logic, latched internally on character boundaries, and combined with the serial dot data to provide monochrome or color video outputs.

The BLANK input defines the active screen area. In color mode, the video outputs are forced to the specified background color when this signal is asserted; in monochrome mode the video outputs are forced to the states defined by the BKGND input, i.e., black if dark background is selected and gray if light background is selected. A separate RBLANK input allows the user to select the amount of border around the active area when operating in color mode or in monochrome mode with light background. This input can be tied high, in which case the area outside the active area will be dark, or it may be pulsed during BLANK periods to externally control the border widths.

In color mode, eight colors for the character (foreground) and eight colors for the background (area other than character) can be selected by the attribute inputs. In monochrome mode, the intensities of foreground and background are a function of the attribute and BKGND inputs, i.e., characters may be black, gray, white, or highlight (very white) while background may be black, gray, or white (see Table 1).

Table 1 MONOCHROME MODE ATTRIBUTE CHARACTERISTICS

REV[1]	AHILT	ABLINK[2]	FOREGROUND VIDEO	BACKGROUND VIDEO
0	0	0	W	B
0	0	1	W/G	B
0	1	0	H	B
0	1	1	H/W	B
1	0	0	B	G
1	0	1	B/W	G/B
1	1	0	B	W
1	1	1	B/H	W/B

NOTES

1 REV = (BKGND) XOR (ARVID):

BKGND	ARVID	REV
0	0	0
0	1	1
1	0	1
1	1	0

2 For blinking, the video outputs are shown as 0/1, where 0 and 1 are the blink timing input states

3 Foreground includes underline when underlining is specified by AUL = 1.

4 When ABLANK = 1, foreground component becomes same as background component.

5 Codes for video outputs are as follows

CODE	TTLV2	TTLV1	BEAM INTENSITY
B	0	0	Black
G	0	1	Gray
W	1	0	White
H	1	1	Highlight

COLOR/MONOCHROME ATTRIBUTES CONTROLLER (CMAC) SCB2675

Preliminary

Character Clock Counter

The character clock counter divides the DCLK input to generate the character clock ($\overline{CCLK}$). The divide factor is specified by the clock control inputs (C1-C0) as follows:

C1	C0	SCB2675B	
		DOTS/ CHAR.	$\overline{CCLK}$ DUTY CYCLE*
0	0	10	5/5
0	1	7	4/3
1	0	8	4/4
1	1	9	5/4

*High/low

C1	C0	SCB2675C	
		DOTS/ CHAR.	$\overline{CCLK}$ DUTY CYCLE*
0	0	10	5/5
0	1	6	3/3
1	0	8	4/4
1	1	9	5/4

*High/low

The number of dot clocks/character is normally the number of dots/character as listed above. However, when dot width control is specified, the DCLK input is divided by two before it is applied to the character clock counter resulting in the number of dot clocks/character being double those listed above, although the number of displayed dots/character remains the same. See Dot Modulation section of this data sheet.

Video Shift Register

On each character boundary, the parallel input dot data (D0-D8) is loaded into the video shift register. The data is shifted out least significant bit first (D0) at the DCLK rate. If 10 dots/character are specified (C1-C0 = 00), the tenth dot will be the same as D8. The serial dot data from the video shift register is routed to the video logic where it is combined with the cursor and attribute control bits to produce the video data outputs.

Mode Select, Attribute and Cursor Control

The mode select logic multiplexes the monochrome and color attribute inputs and outputs as specified by the M/C input. The monochrome mode provides blank, reverse video, highlight and two general purpose attributes. The latter may be used, with external logic, to combine other attributes (e.g., overscore) into the video stream. The color mode provides RGB foreground and background color attributes. Both modes provide double width characters, blink, underline, dot width control and dot stretching.

The cursor and attribute inputs are pipelined internally to allow for system pipeline propagations. The cursor input signal is delayed internally by two $\overline{CCLK}$s (one for RAM and one for the character generator), while the attribute inputs are delayed for one $\overline{CCLK}$ to account for the delay of the character data through the character generator latches. The attribute timing inputs (BLINK, UL and DOTS) are clocked into the 2675 at the beginning of each scan line time by the falling edge of BLANK. Thus, these inputs must be in their proper state at the falling edge of BLANK preceding the scan line where they are required to be active. The BLANK signal itself is also delayed internally to provide for the RAM and character generator delays (see figures 6 and 7). Internal delays cause the video outputs to be delayed relative to $\overline{CCLK}$ as illustrated in figure 8.

Video Logic

Each character block consists of the three components shown in figure 1. Symbol video is generated from the dot data inputs D0-D8. Underline video is enabled by the AUL attribute and is generated during the scan lines for which the UL input is active. Underline and symbol video are always the same intensity or color, and other attributes (e.g., ABLINK) apply to them equally. The combination of underline and symbol video is also referred to as foreground video. Background video is the area of the character block corresponding to the absence of foreground video. The assertion of the non-display attribute (ABLANK) causes the entire character block to be displayed as background.

In monochrome mode, the serial dot data and pipelined cursor and attributes are combined to generate four video intensities (black, gray, white and highlight) which are encoded on the TTLV1 and TTLV2 outputs as follows:

TTLV2	TTLV1	VIDEO INTENSITY
0	0	Black
0	1	Gray
1	0	White
1	1	Highlight

Table 1 describes the relationship between attributes and video intensity of the foreground and background components of the character block in monochrome mode.

In color mode, the colors of the foreground and background components are specified by the corresponding attribute inputs; AREDF, AGREENF and ABLUEF dictate the color of the foreground component while AREDB, AGREENB and ABLUEB do the same for the background component. In this mode, the serial dot data and pipelined cursor and attributes are combined to generate four video outputs. The RED, GREEN and BLUE outputs separately contain the corresponding foreground and background components. The LUM output is the logical-OR of the foreground colors and can be used to drive a separate monochrome monitor or to select a different set of colors for the foreground.

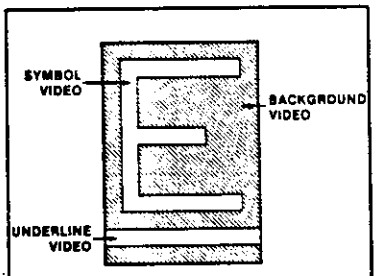


Figure 1. Character Block Definition

COLOR/MONOCHROME ATTRIBUTES CONTROLLER (CMAC) SCB2675

Preliminary

Dot Modulation Logic

The dot modulation logic controls the video shift register to supply dot stretching and dot width control.

Dot stretching is controlled by the DOTS input which is sampled each scan line at the trailing (falling) edge of BLANK. If DOTS is asserted at that time, all characters on the following scan line will have dot stretching applied. Dot stretching causes an extra dot to be added to individual dots or groups of dots as shown in figures 2 and 3. Dot stretching can be used to:

1. Compensate for low video bandwidth monitors (since the minimum active displayed segment with dot stretching is two DCLKs).
2. Assure crisp black characters when operating in white background mode.
3. Provide thick characters as a means of distinguishing areas of the display.

Dot width is controlled by the DOTM and ADOTM inputs. DOTM is tied either high, which enables the feature on the entire display, or low, which disables the feature. With ADOTM high, the dot width of characters can be selectively controlled by assertion of the ADOTM attribute input. When operating in this mode, the dot clock input is divided by two before being applied to other circuits in the CMAC. This affects the $\overline{CCLK}$ output.

When dot width control is enabled as above, two DCLKs are used for each video dot period. Asserting ADOTM for a particular character will cause each active video dot of the displayed character to be turned on for one DCLK and off for the other DCLK, while if ADOTM is negated for that character, the active video dot for that character will be turned on (black background) or off (white background) for both DCLK times (see figures 2 and 4). Only the character video component of the character block is modulated. Underline video and background are not affected by on-time modulation. Width control can be used to:

1. Make horizontal lines and vertical lines appear the same brightness on the display.
2. Provide two different brightness levels for characters without requiring a monitor with analog brightness inputs.

However, note that the effects produced by this feature are highly dependent on the video amplifier characteristics of the monitor used.

Double Width Logic

The double width logic controls the rate at which dots are shifted through the video shift register. When the ADOUBLE input is asserted, the associated character video will be shifted at one half the DCLK rate, and the dot information for the next character will be loaded into the shift register two $\overline{CCLK}$s later. The $\overline{CCLK}$ output is not affected. If a double width character is specified at the last location of a character row, the second half of the double width character (one $\overline{CCLK}$) will extend into the horizontal front porch.

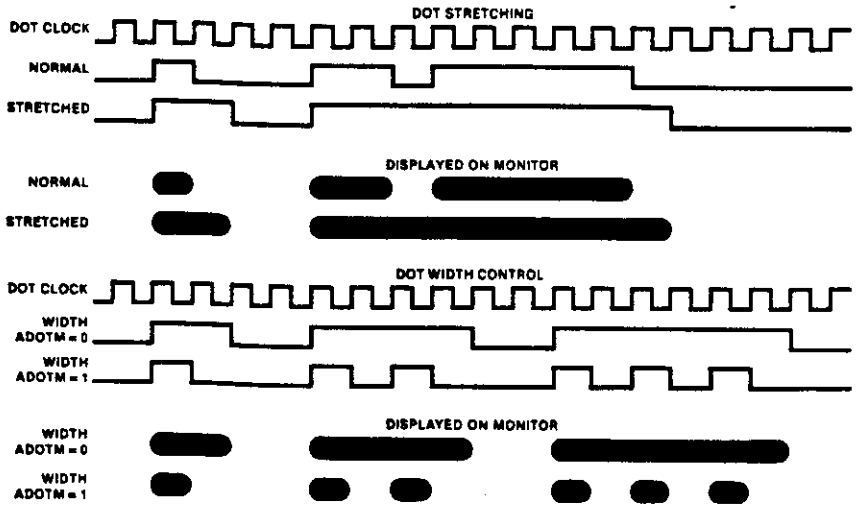


Figure 2. Dot Modulation Timing

COLOR/MONOCHROME ATTRIBUTES CONTROLLER (CMAC) SCB2675

Preliminary

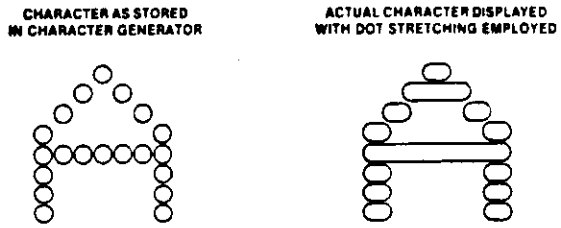


Figure 3. Dot Stretching

Figure 4. Dot Width Control

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
All voltages with respect to ground[3]	−0.5 to +6.0	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, V_{BB} = figure 5[4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2.0			V
V_{OL}	Output low voltage	$I_{OL} = 4mA$			0.4	V
V_{OH}	Output high voltage	$I_{OH} = -400\mu A$	2.4			V
I_{IL}	Input low current	$V_{IN} = 0.4V$				
	DCLK				−800	μA
	All other inputs				−400	μA
I_{IH}	Input high current	$V_{IN} = 2.4V$				
	DCLK				40	μA
	All other inputs				20	μA
I_{CC}	V_{CC} supply current	$V_{IN} = 0V$, V_{CC} = max			80	mA
I_{BB}	V_{BB} supply current	Figure 5			120	mA

COLOR/MONOCHROME ATTRIBUTES CONTROLLER (CMAC) SCB2675

Preliminary

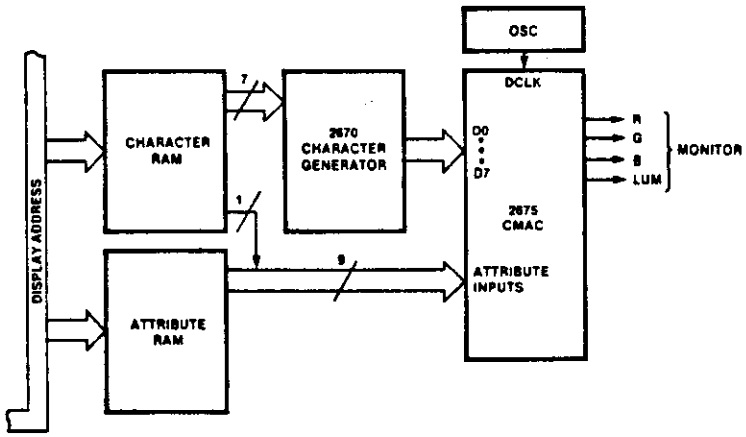


Figure 11. System Block Diagram of SCB2675 in Color Mode

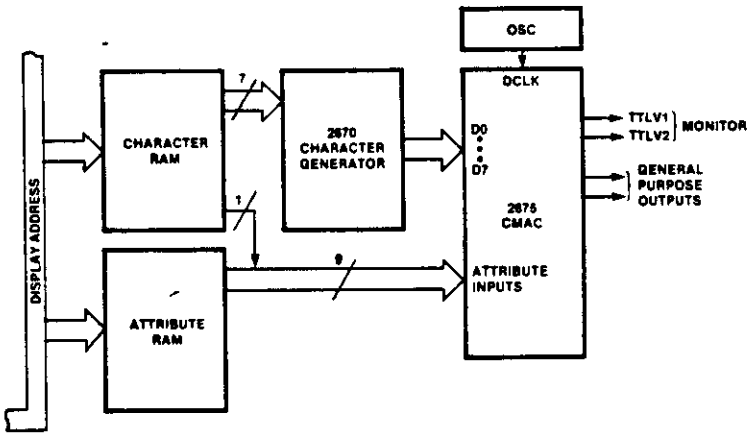


Figure 12. System Block Diagram of SCB2675 in Monochrome Mode

CRT PALS

NAME	DEVICE	COMMENTS
CRT BOARD		
CRT-01AA-M41	14L4	MAP DECODER, 1st Level Decode
CRT-02AA-M37	12L6	MAP DECODER, 2nd Level Decode
CRT-03AA-M38	12L6	BUS CYCLE TIMING CONTROLLER
CRT-04AA-M50	10L8	CHARACTER DISPLAY RAM ARBITOR
CRT-05AA-M46	12L6	I/O BUS TIMING & INTERRUPT CONTROLLER
CRT-06AB-M36	16R4	INTERRUPTER A
CRT-07AB-M45	16R4	INTERRUPTER B
CRT-08AA-M58	14L4	DISPLAY OUTPUT ENCODER
CRT-09AA-M40	14L4	ADDRESS MODIFIER DECODER